Bennett and Landauer clocking in quantum-dot cellular automata

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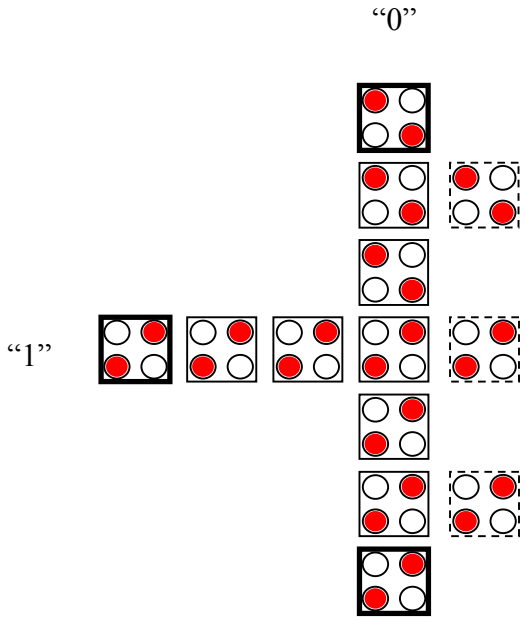
Quantum-dot cellular automata (QCA) is a new computation paradigm which encodes bit information by charge configurations. No current flows through the cells; only Coulomb interaction contributes to the computation. Power dissipation has become an important issue in nanotechnology because of the high densities in nano-devices. The chip will melt unless the device dissipates only a small amount of energy to the environment. Landauer [1] has proposed an adiabatic switching method, which has been applied widely in clocked QCA cells [2]. Gradual clocking insures the cells always in the instantaneous ground state, which can provide arbitrarily low power dissipation if the switching process is slow enough. Non-dissipative computation can be achieved by keeping a copy to the bits that are going to be erased [2]. Bennett pointed out that any computation could be rendered into reversible format by accumulating a history of all information that would normally thrown away, then disposing this history by the reverse of the process that created it [3]. In this paper, we employ the Bennett clocking design in QCA circuits, which clocks the circuit forward through the cell array and then retreats the clock in a backward sequence. In conventional CMOS considerable overhead in circuit complexity is required to achieve Bennett clocking. In QCA by contrast, no additional circuit complexity is required—only a different clock signal. We show by direct calculation of the equations of motion for a QCA system that energy dissipation less than $k_B T \log(2)$ is possible for logically irreversible systems using the Bennett clocking approach.

[1] R. Landauer and R.W.Keyes,IBM J. Res. Dev.14,2 (1970)
[2] J.Timler, C.S.Lent, Journal of Applied Physics 94,(2003)
[3] C. H. Bennett, IBM Journal of Research and Development, 44,1/2 (2000)

A full journal publication of this work will be published in the Journal of Computational Electronics.

(a)



(b)

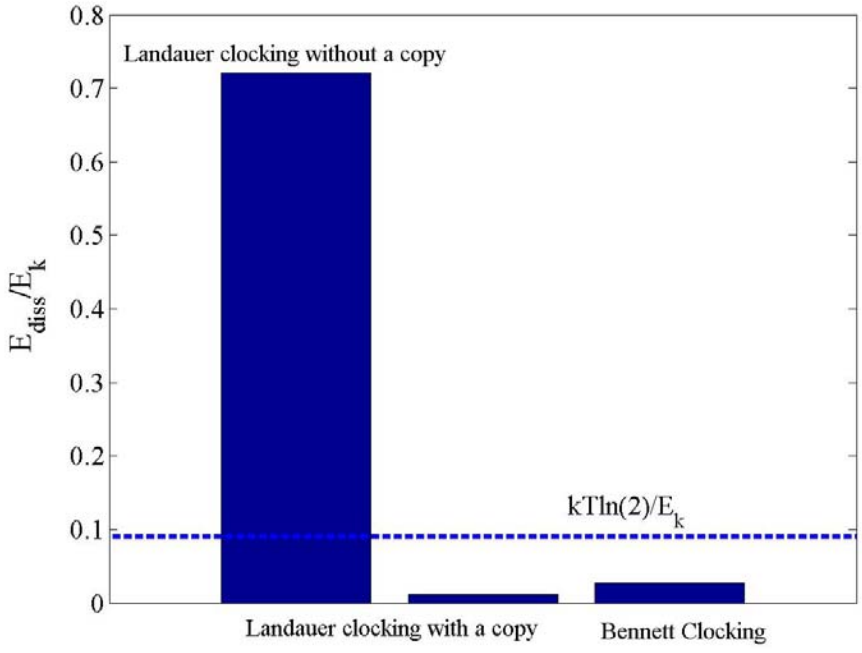


Figure 1: (a) The schematic of a majority gate with fixed inputs. The thicker lines describe the driver cells. The cells with dashed lines imply the copy of the bits. (b) Comparison of the energy dissipation in Landauer clocking without a copy to the erased bit, with a copy to the erased bit and Bennet clocking.

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