Subthreshold Mobility Extraction for SOI-MESFETs

T. Khan, D. Vasileska and T. J. Thornton
Arizona State University, Tempe, AZ, 85287-5706, USA
Fax: (480) 965-8058, Phone: (480) 727-7522
ktk@asu.edu, vasileska@asu.edu, t.thornton@asu.edu

Micropower circuits based on sub-threshold MOSFETs are used in a variety of applications ranging from digital watches to medical implants. The principal advantage of sub-threshold transistor operation is the minimal power consumption, but the main drawback is it's speed, i.e. micropower circuits are limited to operating frequencies below ~ 1MHz due to low cut-off frequency $f_T=\mu V_T/2\pi L_g^2$, where μ is the carrier mobility, $V_T=kT/e$ the thermal voltage and L_g is the gate length. In the sub-threshold regime, it is impractical to increase f_T by reducing the gate length because of difficulties with transistor matching. The only remaining option to increase f_T is to increase the carrier mobility. A candidate structure is the SOI-MESFET or the Schottky junction transistor[1] (SJT) that is currently being fabricated and theoretically characterized within our group. From the simulated mobility results shown in Fig.2 it is found that, in the sub-threshold regime, the SJT[1] (or the SOI MESFET architecture) exhibits higher mobility (5 ~ 10 × larger in weak inversion regime) with respect to conventional SOI MOSFETs. However, the method that we have used to calculate these mobility data is drift based and one can argue that the current conduction in the subthreshold regime is diffusion dominated. Hence, the purpose of this paper is to extract the diffusion based mobility in SJT at low bias conditions to validate the drift-based results. To extract the diffusion coefficient for the SJT[1] using our in-house 2D Monte Carlo device simulator, the following formulation is being used[2],

$$\begin{aligned} D &= \langle \delta x(t)\delta v(t)\rangle = \langle (x(t)-\langle x\rangle)(v(t)-\langle v\rangle)\rangle \\ &= \frac{1}{N}\sum_{i=1}^{N}(x_i(t)-\langle x\rangle)(v_i(t)-\langle v\rangle) \end{aligned}$$

where $\delta x(t)$ and $\delta v(t)$ are the fluctuations of the particle position and velocity with respect to their ensemble averages. Using the above mentioned method we found that the simulated bulk diffusion coefficient is very close to the experimental values[3] (see Fig.1a). Also, using the Einstein relation for non-degenerate semiconductors, we find that the corresponding low-field mobility values are on the order of 951 ~ 1121cm^2/V-sec and confirm the drift based mobility calculation in the subthreshold region (Fig.1b). Therefore, the mobility enhancement in SJT is being confirmed by two different but consistent methods, suggesting that this device structure exhibits higher cut-off frequency, which will make it suitable for application in r.f. micropower circuit design. At the conference, we will also present the output characteristics and the gate-length variation of the cut-off frequency of several SJT we have fabricated, measured and simulated within the Nanostructures Research Group at Arizona State University.

---

[1] T. J. Thornton "Physics and Applications of the Schottky Junction Transistor", IEEE Trans. Electron Devices 48, 2421 (2002).

[2] C. Jacoboni and P. Lugli, The Monte Carlo method for semiconductor device simulation. Wein , New York : Springer-Verlag, (1989)

[3] C. Jacoboni and L. Reggiani, "The Monte Carlo Method for the Solution of Charge Transport in Semiconductors with Applications to Covalent Materials", Rev. Modern Phys., 55, 645 (1983).

A full journal publication of this work will be published in the Journal of Computational Electronics.

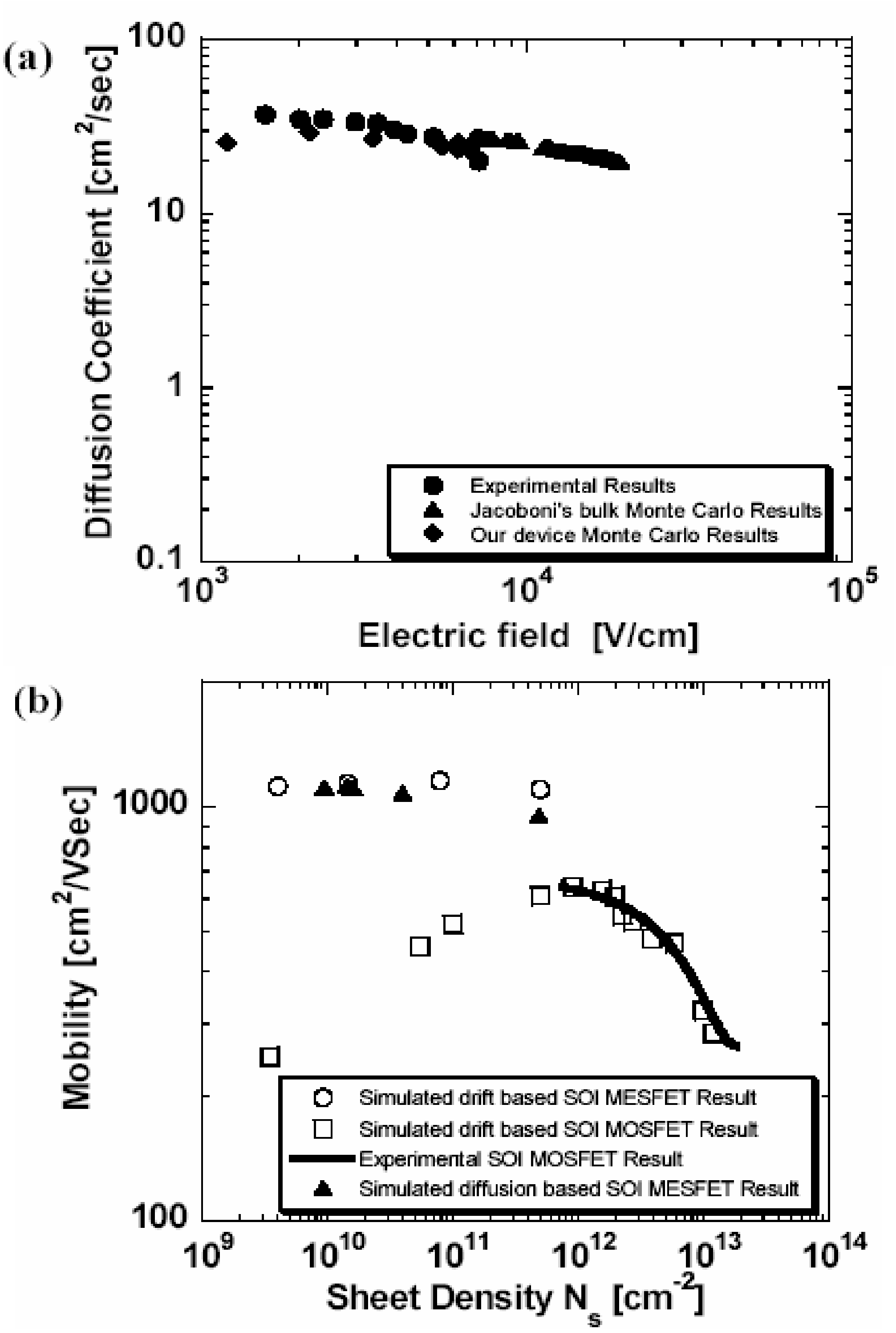

Figure 1: (a) Diffusion coefficient vs. Electric field in bulk Si samples. Notice the excellent agreement between the experimental values and our simulation results (top figure). (b) Mobility vs. sheet density extracted from both drift and diffusion technique. Also shown here are the universal mobility results for SOI MOSFETs (bottom figure).

A full journal publication of this work will be published in the Journal of Computational Electronics.