Investigation of Electrostatic Discharge Characteristics on Low Temperature Polycrystalline Silicon Thin Film Transistors

Jam-Wem Lee[1], Yiming Li[1,2,*], and Hsiao-Yi Lin[3]
[1]Department of Computational Nanoelectronics, National Nano Device Laboratories
[2]Microelectronics and Information Systems Research Center, National Chiao Tung University
[3]Toppoly Optoelectronics Corp.
[*]Corresponding Author. P.O. BOX 25-178, Hsinchu 300, TAIWAN; Email: ymli@faculty.nctu.edu.tw

In this paper theoretical and experimental examinations have been performed for exploring electrostatic discharge (ESD) characteristics in low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs). It is found that LTPS TFT is greatly damaged during ESD current. The damage is quite different from those devices that fabricated on single crystalline silicon films. A short circuit characteristic is found for single crystalline silicon devices; however, an open circuit behavior for polycrystalline transistors is observed. The difference may due to effects of grain boundaries and poor thermal conductivity.

Excimer laser annealing technique has recently been proposed in fabrication of LTPS; in particular for its applications to active-matrix liquid crystal display [1-3] and achieving system on panel. Compared with traditional TFTs, one of the most attractive properties of the laser annealed polycrystalline silicon is mainly due to its relatively larger grain size and higher electron-hole mobility. Therefore, embedded driving circuits could be easily achieved for replacing additional driving integration circuits in LCDs. It is known that ESD protection circuits play an important role in realizing the embedded driving circuit by using laser annealed LTPS TFTs. However, from practical application point of views, ESD protection circuits designed by LPTS TFTs has seriously faced the weakened ESD robustness problem [3].

To study the problem of weakened ESD robustness for embedded protection circuits, LTPS TFTs in this work are fabricated, measured, and computationally analyzed. Result shows that a bad thermal conductivity enhances the electro - migration of silicon atoms. It leads to a quite different mechanism of ESD failure in comparison with single crystalline devices. In contrast with the short circuit in the single crystalline devices, an open circuit is found in LTPS TFTs.

Shown in Fig. 1, LTPS TFT devices are fabricated on the glass substrate by using the novel excimer laser annealing process [1-2]. A 50 nm amorphous silicon film is firstly deposited by using a PECVD cluster tool at 300oC. The silicon film is then taken into a novel excimer laser system and transfers the amorphous silicon into the large grained poly crystalline silicon. The key process improves the mobility of both electrons and holes. After the source/drain formatted using the high power plasma implantation, a 100 nm oxide is deposited by using the TEOS source in PECVD clusters. Gates, contacts, and interconnections are finally deposited and etch to have a good electrical connection between the designed TFTs. The current versus voltage (IV) characteristics are measured by using transmission line pulse system, which generates 100 ns pulses and corresponds to the human body mode standard [1-3]. To theoretically study the failure mechanism among samples, simulation is performed by our own HD device simulator [3], where the grain size, grain boundary, lattice temperature, and electro - migration of silicon atoms are modeled in our simulation.

Shown in Fig. 2, preliminary IV characteristics of both n-channel and p-channel LTPS TFTs are measured. Firstly, comparison between Fig. 2a and Fig. 2b shows that there is a significant IV characteristics difference between single crystalline devices and LTPS TFTs. Fig. 2a indicates the main difference between nFET and pFET, where the nFET has a relatively low resistance before the device going into failure. By theoretical analysis, the result is caused from the

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hole-accumulation in nFETs. The turn-on characteristics for nFET and pFET are very different; however, these two devices have a similar failure behavior under same discharge current. We conclude that the open circuit phenomenon, shown in Fig. 2a, is mainly caused from the electro-migrations of silicon atoms. Effects of electro-migration are dominantly proportional to the current density and device temperature, so both devices have similar characteristics under electrostatic discharge.

In this paper, we have found that the electro-migration plays an important role for designing ESD protection circuits by LTPS TFTs. Reduction on electro-migration effect will play an effective way to improve ESD robustness for LTPS TFT protection circuits. Details of modeling and simulation for the aforementioned experimental characteristics will be discussed afterward.

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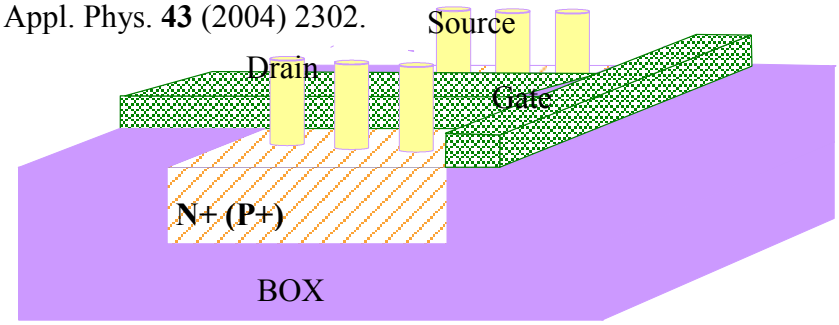

Figure 1. A three-dimensional illustration of the explored LTPS TFTs.

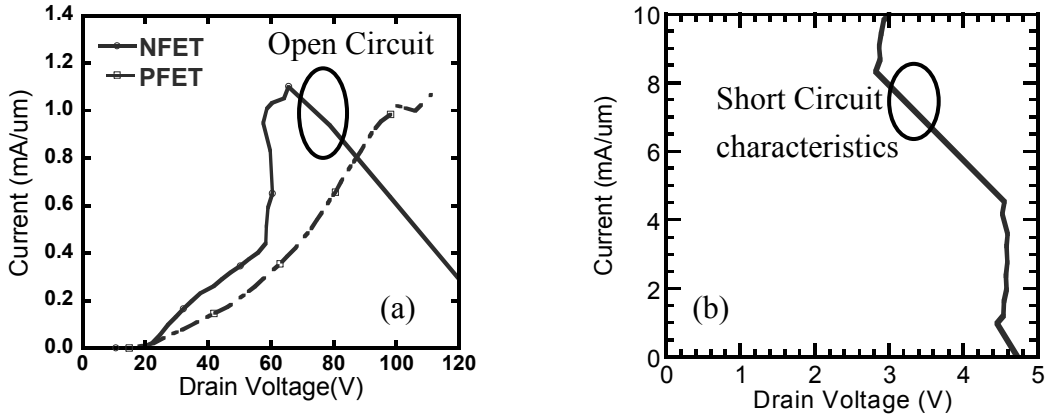

Figure 2. The ESD characteristics of (a) 4.5 μm n-channel and p-channel LTPS TFTs and (b) single crystalline 90 nm SOI nFET.