TCAD ready density gradient calculation of channel charge for Strained Si/Strained $Si_{1-x}Ge_x$ dual channel pMOSFETs on (001) Relaxed $Si_{1-y}Ge_y$

C. D. Nguyen†, A. T. Pham, C. Jungemann and B. Meinerzhagen
NST, TU Braunschweig, Postfach 33 29, 38023 Braunschweig, Germany
†Phone: +49 531 391 3168, Fax: +49 531 391 8189, E–mail: c-d.nguyen@tu-bs.de

Introduction: The dual channel MOSFET with strained $Si/Si_{1-x}Ge_x$ layers on relaxed $Si_{1-y}Ge_y$ (see Fig. 1) is a promising structure for the improvement of CMOS performance because of its enhanced carrier mobilities [1]. In order to obtain the correct threshold voltage and gate capacitance of these devices, it is essential to accurately model the channel charge distribution. First, the size quantization of the two-dimensional hole gas (2DHG) caused by the carrier confinement in the strained layers is evaluated based on the Schrödinger equation with an adequate description of the valance band structure using the $\mathbf{k}\cdot\mathbf{p}$-method (KPSE). The CV-curves for these devices have been calculated by solving the KPSE and Poisson's equation self-consistently. Based on these results, the valence band offsets required for modeling the problem with the simpler and more efficient density gradient model (DGM) [2] are extracted. It is shown that with the extracted parameters the DGM achieves accurate results independent of the thickness of the strained Si layer.

Simulation Models: Size quantization in z-direction (perpendicular to the hetero interfaces) is well described by an one dimensional Schrödinger equation using the standard 6×6 $\mathbf{k}\cdot\mathbf{p}$-method [3,4]. The quantum-mechanical contribution to the charge density is calculated based on the eigen solutions of the KPSE for all relevant points in the two-dimensional $\mathbf{k}=(k_x,k_y)$ space. In contrast to [5], a modified discretization scheme for the two-dimensional $\mathbf{k}=(k_x,k_y)$ space is used. Moreover, the CV-curves for mobility and band-offset extractions are determined by 1st order perturbation theory. The combined effect of both algorithmic improvements is a factor of 10 less CPU-time.

Application of the DGM as implemented in commercial TCAD suites requires certain material-dependent parameters. Some of these parameters can be determined in a straightforward manner from theory, like the effective density of states for strained SiGe. Other quantities, like the band offsets at hetero interfaces, have a different meaning in the DGM compared to the more fundamental KPSE. In the KPSE the band offsets are implicitly included and depend on the wave vector. For the DGM on the other hand effective band offsets independent from the wave vector are required, which can be obtained by matching CV-curves [6].

Results: In our study a dual channel MOSFET (see Fig. 1) with an n-type substrate doping of $5\cdot 10^{17}/cm^3$ and a metal gate is investigated. The confinement of the holes to the strained SiGe region depends on the gate bias. In Fig. 2 the resultant hole density is shown and for a gate bias of -2V nearly all holes are found in the strained SiGe layer where the mobility is high. At a gate bias of -4V the total number of holes increases, but most of the holes are now located in the strained Si region where the mobility is lower.

The band offsets $\Delta E_v^{I/II}$ and $\Delta E_v^{II/III}$ have been extracted based on the CV-data calculated by the KPSE (250meV and 450meV, respectively). These values differ by 16 and 54meV from the values determined from theory (see [7]). In Fig. 3 good agreement is found between the DGM and KPSE for the newly extracted band offsets. The small error in strong inversion, where the influence of the band offset $\Delta E_v^{I/II}$ can be neglected, is caused by the incomplete description of size quantization effects by the DGM. To demonstrate that the new band offsets can be used independent of the thickness of the strained Si layer, CV-data calculated by the KPSE and the DGM are shown in Fig. 4 for a hetero structure with a thicker strained Si layer. The results confirm the reliability of the new band offsets.

Conclusions: For the first time accurate CV-characteristics for strained Si/SiGe dual channel pMOSFETs are calculated based on the density gradient method. These results make the direct

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application of commercially available TCAD tools feasible for the calculation of CV characteristics of such complicated structures.

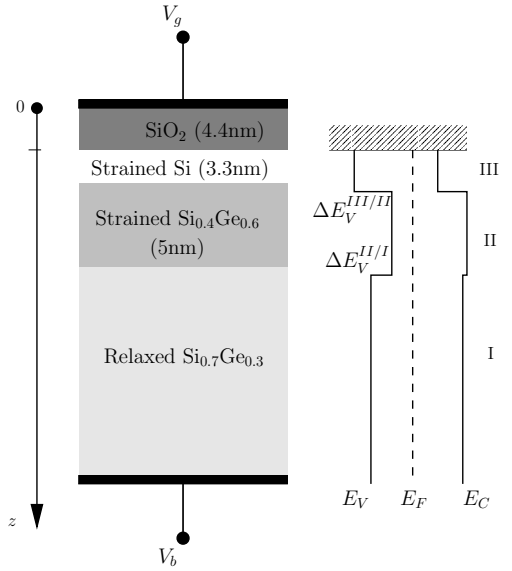

Fig. 1 Layer structure and band alignment for strained Si/strained $Si_{0.4}Ge_{0.6}$ dual channel MOSFET on relaxed $Si_{0.7}Ge_{0.3}$.

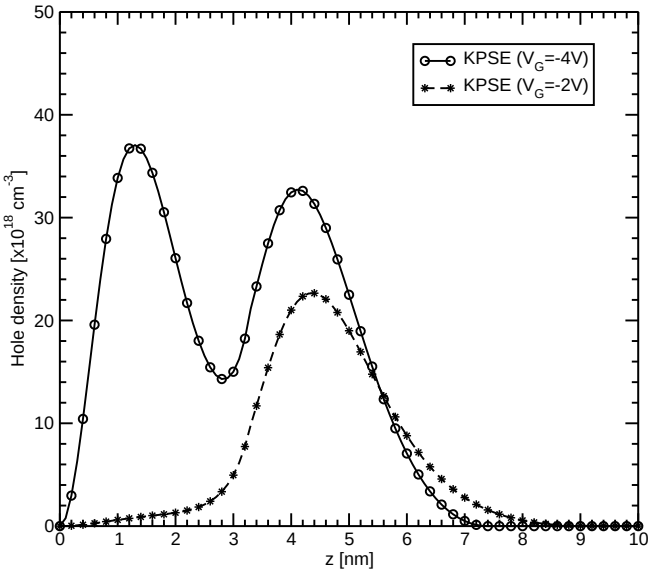

Fig. 2 Hole density at room temperature for two gate biases evaluated by KPSE.

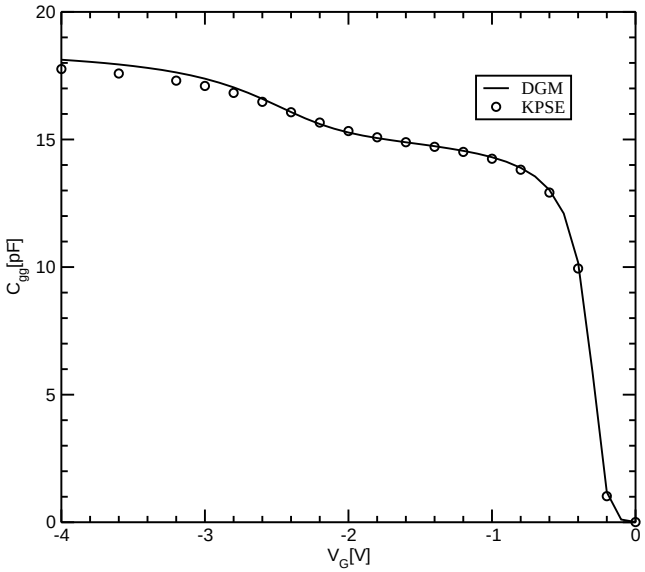

Fig. 3 Gate capacitance of the hetero structure at room temperature where the thickness of the strained Si region is 3.3 nm.

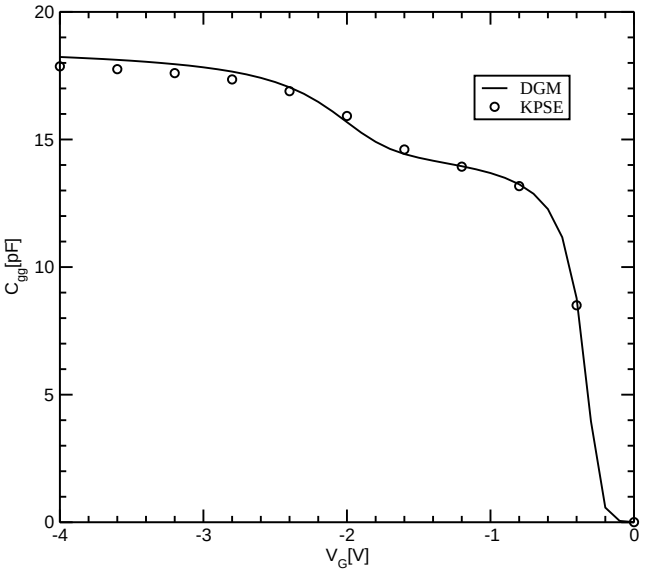

Fig. 4 Gate capacitance of hetero structure at room temperature where the thickness of the strained Si region is 4.0 nm.

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