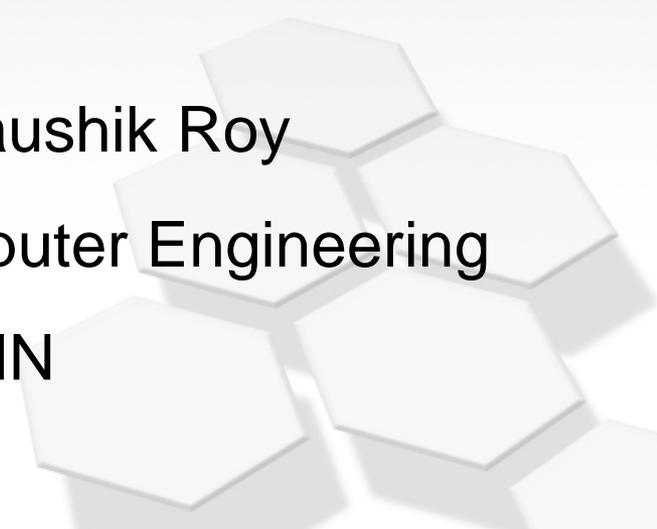


# **Circuit Modeling of Carbon Nanotubes and Their Performance Estimation in VLSI Design**

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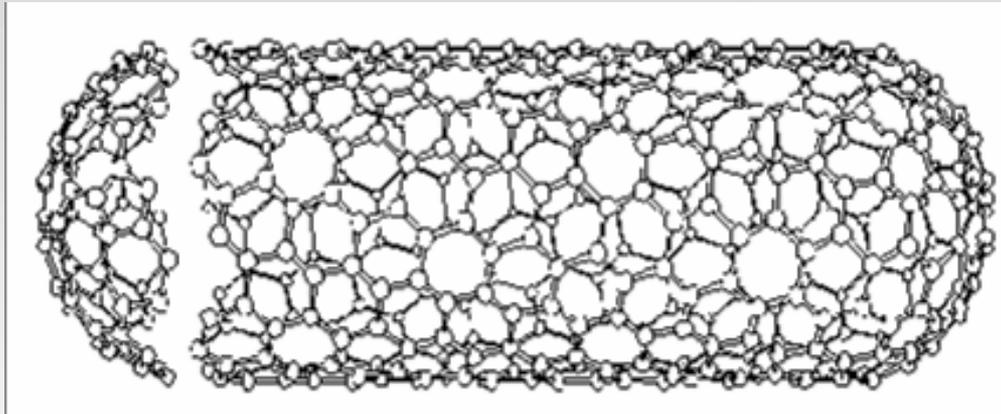
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# Overview

- Introduction to carbon nanotubes and carbon nanotube FETs.
- Metallic CNTs as possible interconnect solution.
- An RLC model of metallic CNTs.
- Simulations and performance predictions.
- Metallic CNTs vis-à-vis Cu.
- Pros and Cons of CNT interconnects.



# Carbon Nanotubes



Carbon nanotubes are graphite sheets rolled in the form of tubes.

- Satisfied C-C bonds
- Mechanically strong
- Electrically quasi 1D transport close to the ballistic limit

Source: IBM

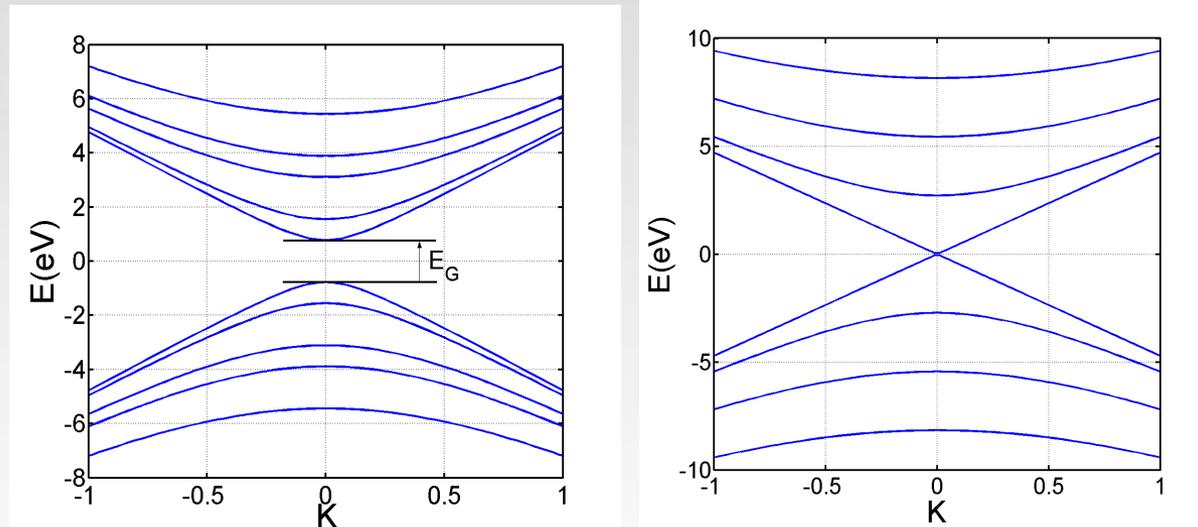


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# Semiconducting and Metallic CNTs

## Chirality determines the nature of the CNT



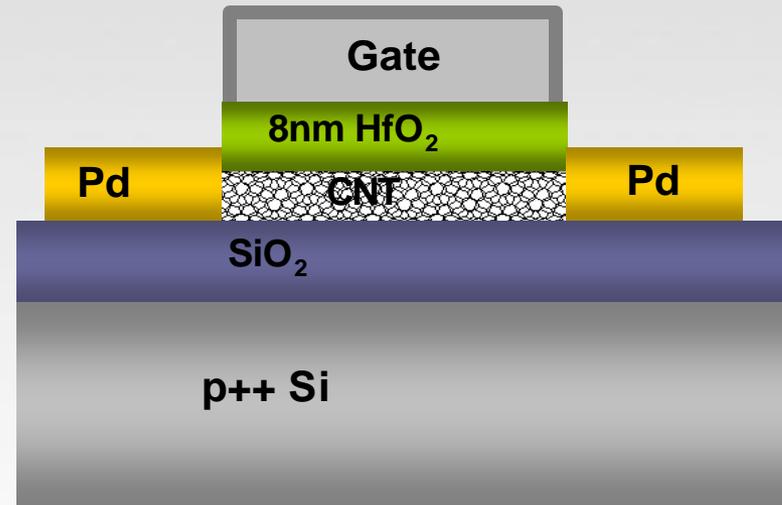
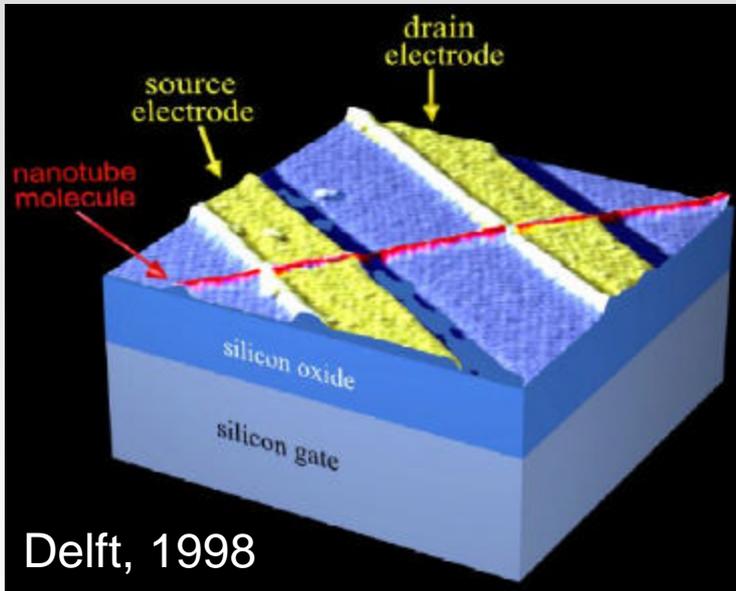
- Typical diameters are  $\sim 0.6\text{nm}$  to  $3\text{nm}$ .
- The bandgap of semiconducting nanotubes is inversely proportional to the diameter.
- The metallic counterparts are studied for interconnects/vias.



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# The semiconducting CNT: CNTFETs 1998 - 2004



Delft:  
Tans, et al., *Nature*, **393**, 49, 1998

IBM:  
Martel et al., *APL*, **73**, 2447, 1998

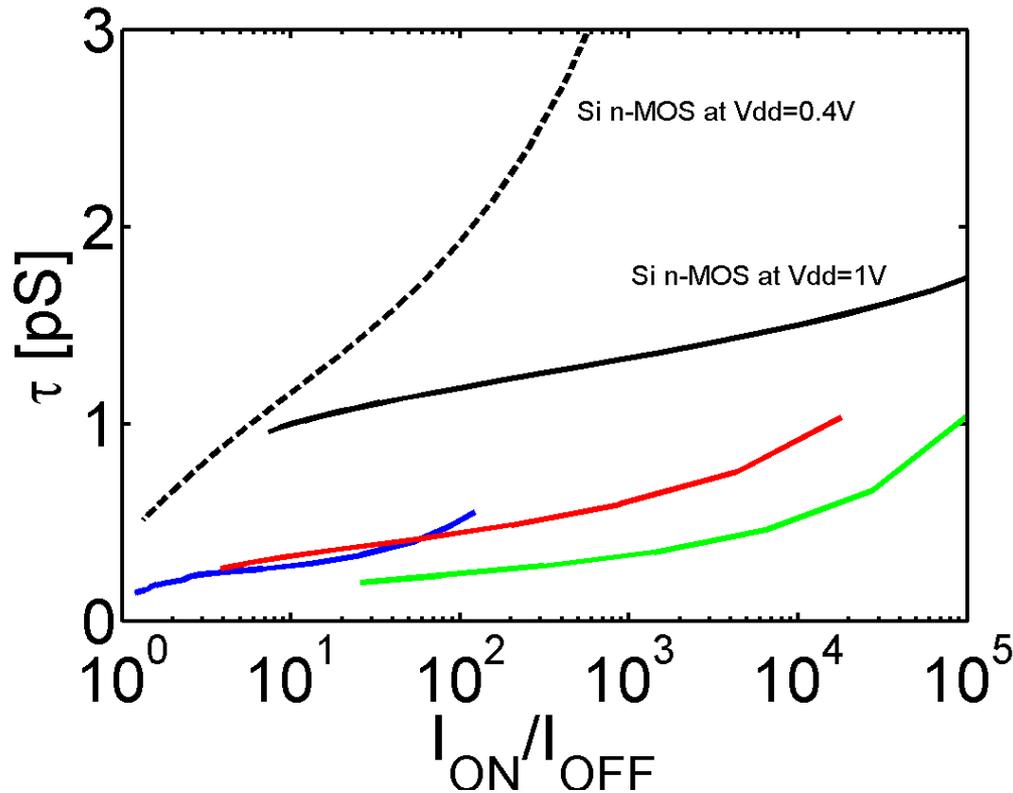
Javey, et al., *Nano Letters*, **4**,  
1319, 2004



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# Performance Prediction: CNTFETs vs. Si MOSFETs



**CNTFETs ( $V_{DD} = 0.4V$ )**

**p-CNT SBFET (Javey)**

**p-CNT SBFET (projected)**

**CNT MOSFET (projected)**

$$t = C_G V_{DD} / I_{ON}$$

Si n-MOS data is 70 nm  $L_G$  from 130 nm technology  
from Antoniadis and Nayfeh, MIT

# Motivation for CNT Interconnects

- An **all CNT design**.
- Parasitics will play an important role as the intrinsic gate capacitance is extremely small.
- Ultra-small and high reliability.
- Cu can handle a max. current density of  $\sim 10^6 \text{ A/cm}^2$  whereas CNTs can handle more than  $10^8 \text{ A/cm}^2$ .
- Mechanically strong and no observable electro-migration effects.



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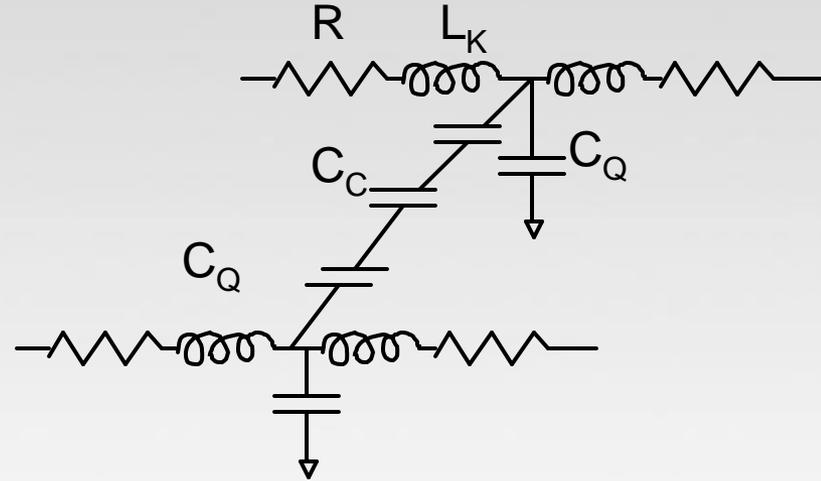
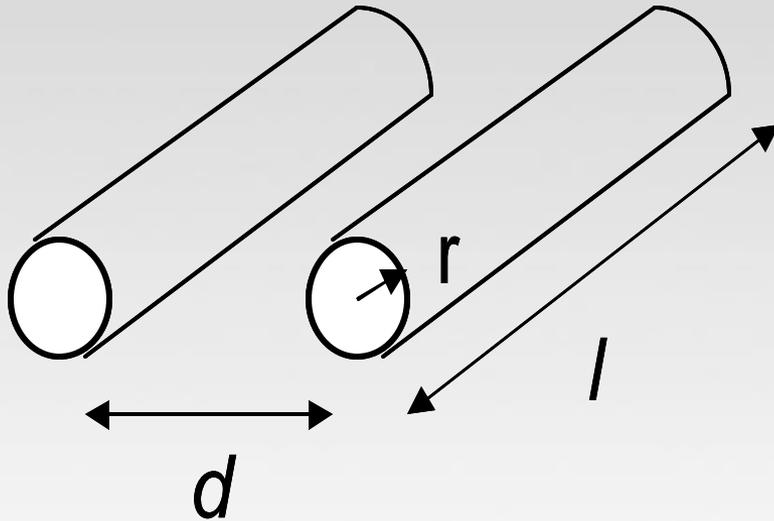
# What are its implications in digital VLSI?



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# Modeling CNT Interconnects



## RLC Model for CNT Interconnects:

- Model the scattering dependant resistance
- Incorporates quantum as well as electrostatic capacitances
- Models the kinetic (or self) inductance



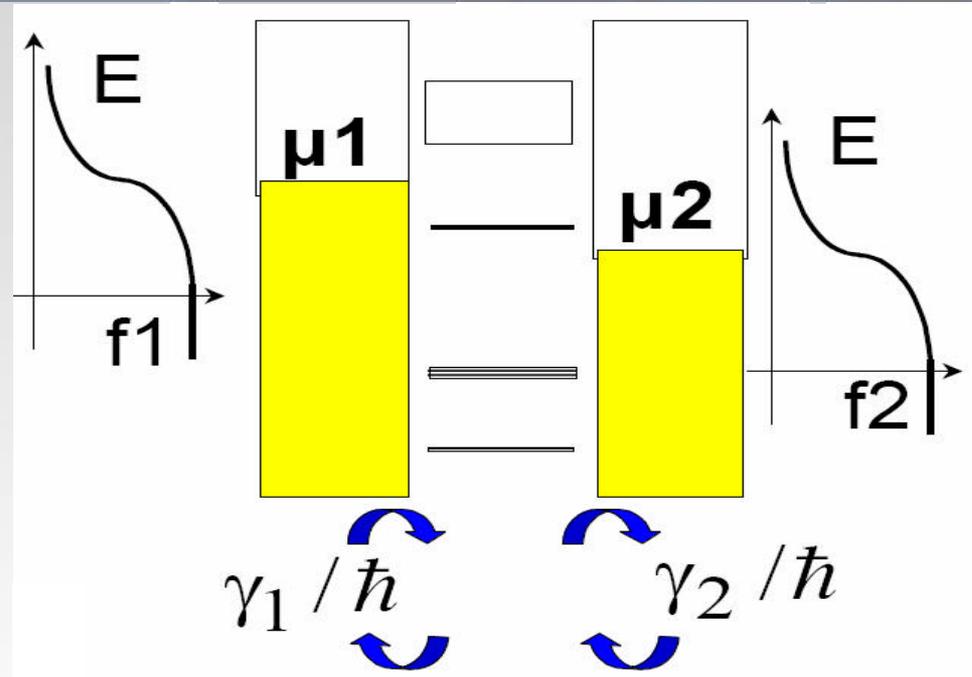
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# Nanoscale conduction

Left contact pours in electrons and the right contact drains them out

- ? is the coupling coefficient



$$I_{left} = q \frac{g_1}{\hbar} [f_1 - N]$$

$$I_{right} = q \frac{g_2}{\hbar} [N - f_2]$$

$$\longrightarrow I = \frac{q}{\hbar} \frac{g_1 g_2}{g_1 + g_2} [f_1 - f_2]$$

Can current increase indefinitely with increasing ??



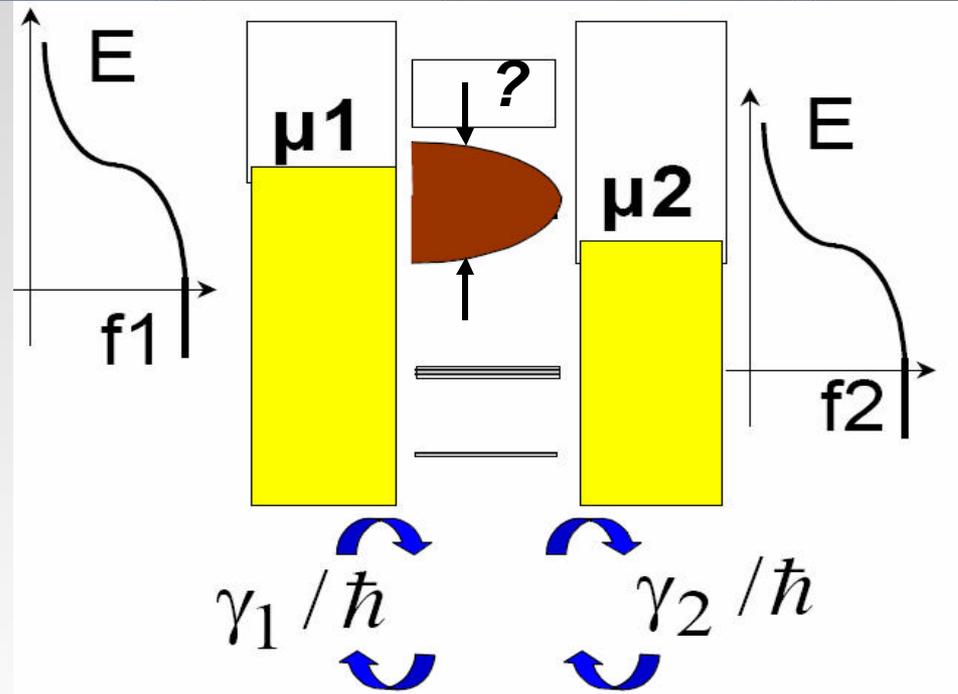
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# Energy Broadening

The energy level broadens when in contact with a metal.

$$I = \frac{q}{\hbar} \frac{g_1 g_2}{g_1 + g_2} \frac{qV}{g_1 + g_2}$$



Maximum conductivity for one mode of transport

$$\frac{I}{V} = \frac{2q^2}{\hbar} \sim \frac{1}{13K\Omega}$$



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# With Scattering..

For  $l >$  the mean free path of phonons

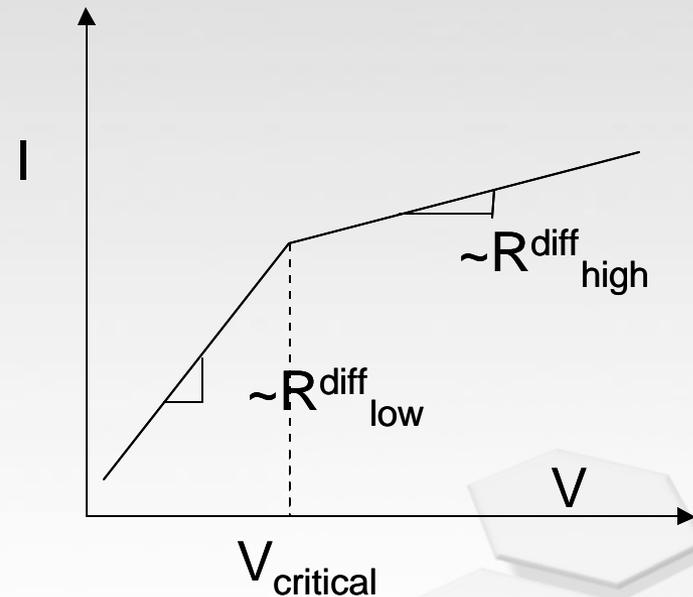
$$R = \frac{dV}{dI} = \left( \frac{h}{4q^2} \right) l$$

For  $V < V_{critical}$

$$\lambda_{acc} \sim 1.6\mu m$$

$V > V_{critical}$

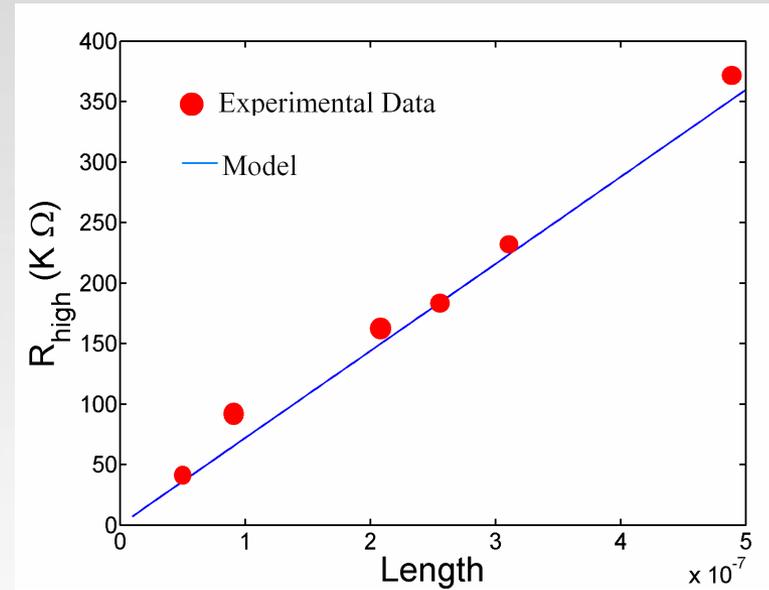
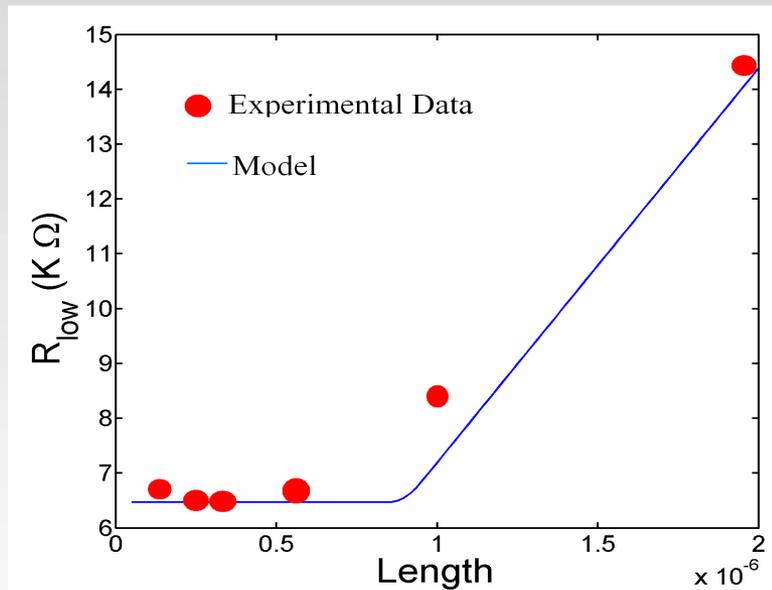
$$\lambda_{op} \sim 200nm \quad \lambda_{zo} \sim 30nm$$



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# Modeling Resistance



Non Linear Resistance Model has been verified with experimental data

*\*Ji-Yong, et. al., cond-mat/0309641, Sept. 28, 2003*

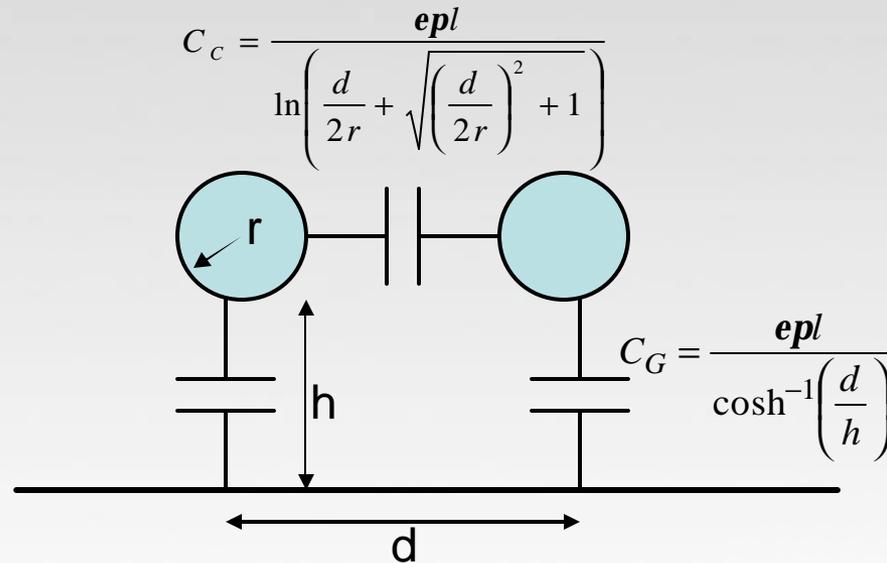


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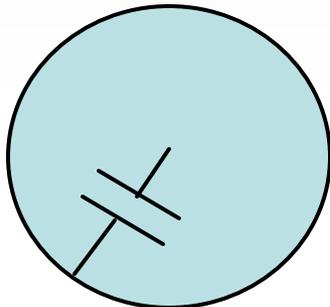
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# Modeling capacitance

Electrostatic capacitance due to presence of nearby ground plane.



The electrostatic model assumes that the wires are equipotential. But due to the low density-of-states potential drops in the wire



$$C_Q = \frac{2q^2}{h\nu_F} \sim 100 \text{ aF}/\mu\text{m}$$

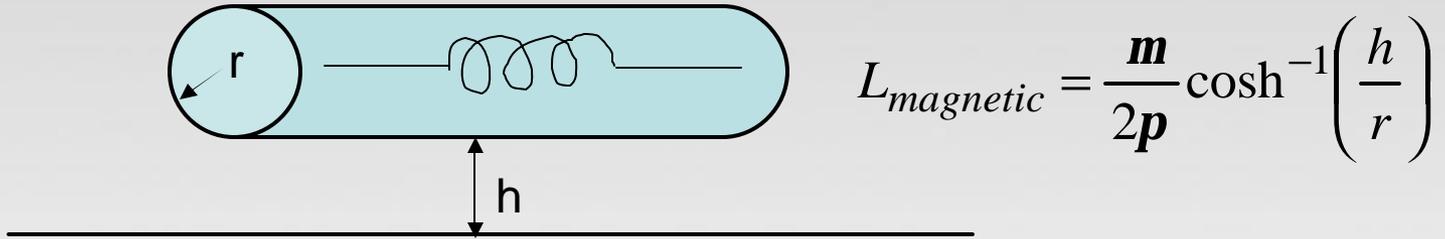
$\nu_F$  is the Fermi velocity in graphite  $\sim 8.1015 \text{ m/s}$



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# Modeling Inductance



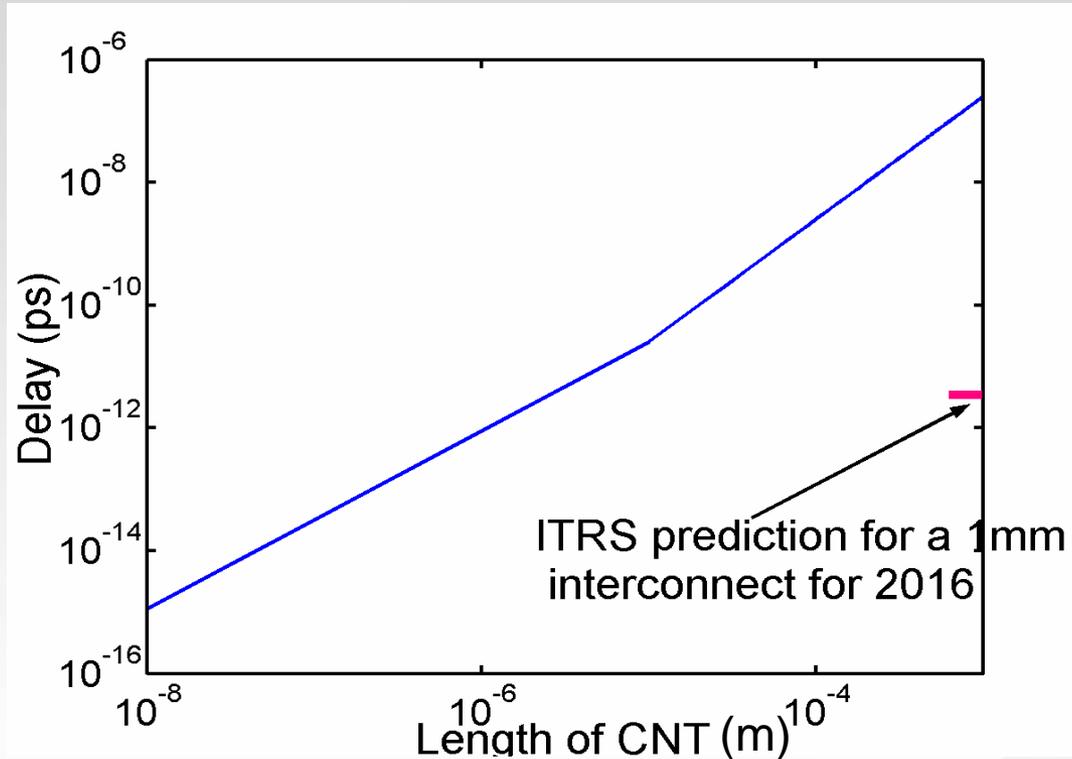
To add to the magnetic inductance we have kinetic inductance due to finite momentum relaxation time of the electrons (significant for 1D electronic transport)

$$L_{kinetic} = \frac{h}{2q^2 v_F}$$

$v_F$  is the Fermi velocity in graphite  $\sim 8 \cdot 10^{15}$  m/s



# Performance of a single CNT: Response to a step input



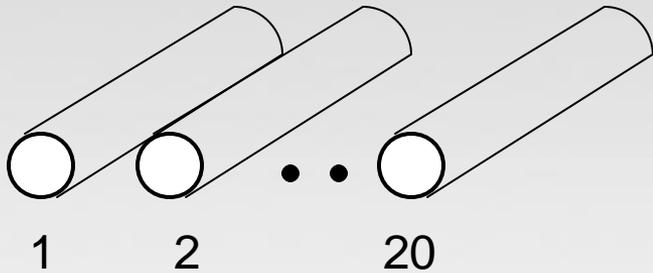
Delay vs length of a single CNT interconnect. The ITRS prediction has been marked.



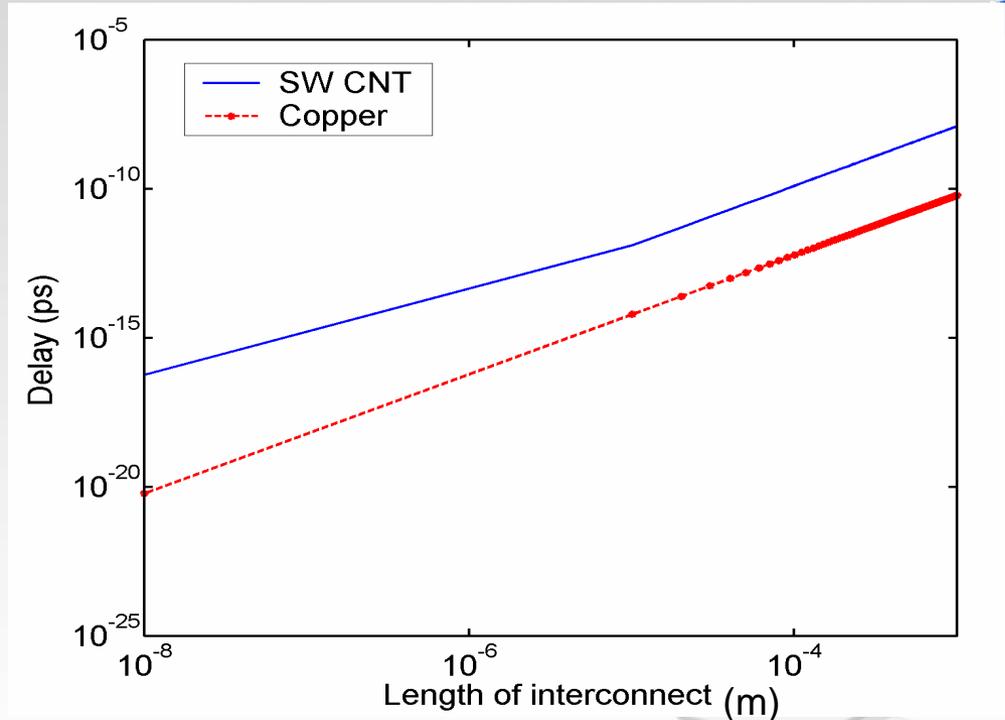
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# Parallel CNTs: Performance estimation



Cu at nanoscaled dimensions will have higher resistivity due to grain boundary and surface scattering



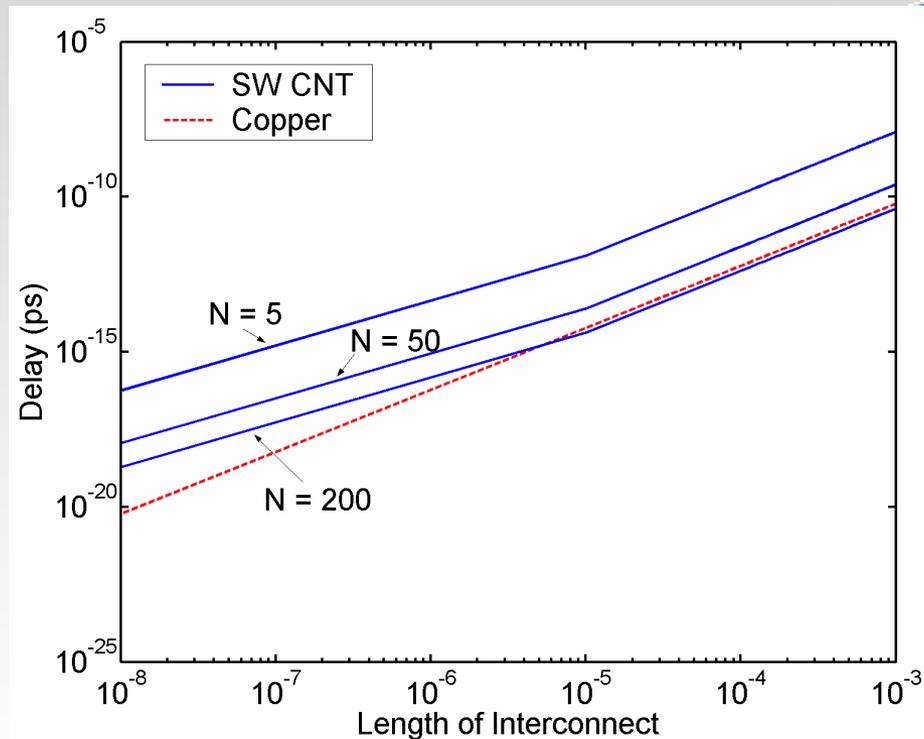
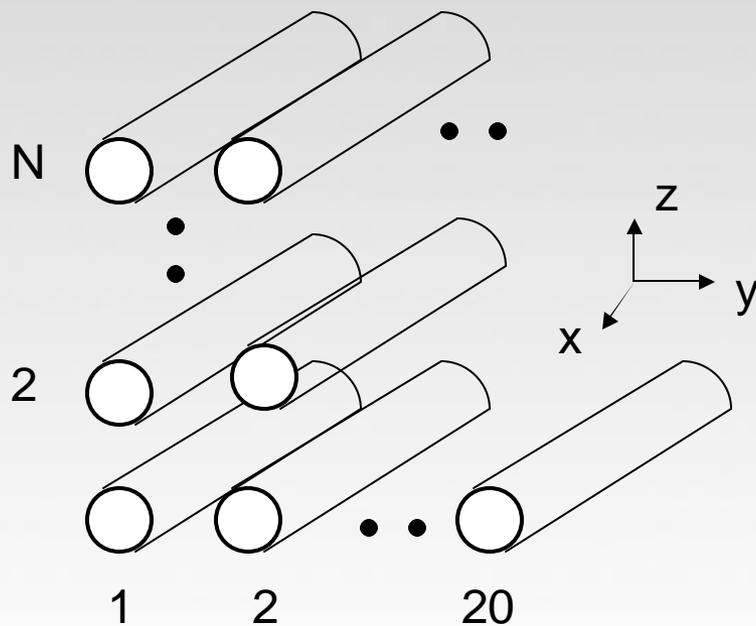
Comparison of delay of 20 parallel CNT interconnects with copper interconnect having the same equivalent width ( $w=80\text{nm}$ ). The height of Cu wire is such that  $J_{\text{MAX}} \sim 10^6 \text{ A}\cdot\text{cm}^{-2}$



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# Stacking in the third dimension



- The height of Cu is such that  $J_{MAX} \sim 10^6$  A.cm<sup>-2</sup>
- We require 200 layers of nanotubes to match the RLC delay of Cu.



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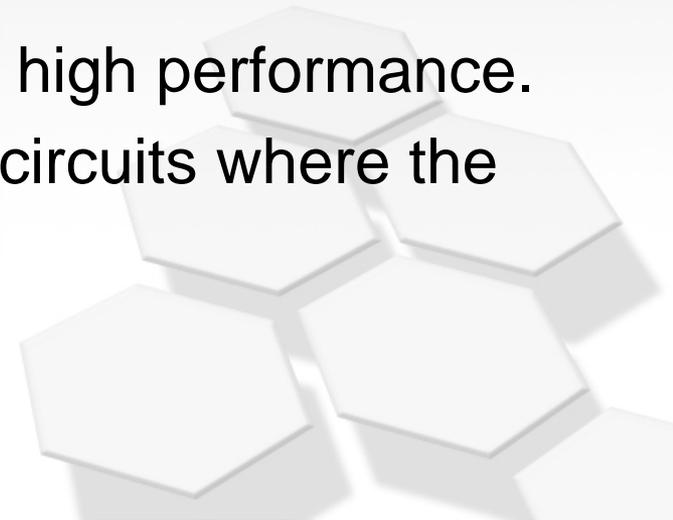
# Observations

- Digital circuits are (most often) voltage driven.
- High current density will not reduce the high RLC delay.
- Longer interconnects suffer severely from scattering. Even for the smaller ones resistance per nanotube  $\sim 6\text{KO}$ .
- Higher frequencies are impeded by kinetic inductance.



# Summary

- CNTs are highly reliable, can endure two-orders of higher current density than Cu.
- Can only be used in relatively slower circuits or in subthreshold operation where the device resistances are high.
- CNT interconnects are severely limited by the contact resistances and kinetic inductance.
- High current densities do not result in high performance.
- Can only be used in relatively slower circuits where the device resistances are high.



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