Full –Band Particle-Based Analysis of Device Scaling For 3D Tri-gate FETs

By

P. Chiney

Electrical and Computer Engineering Department,
Illinois Institute of Technology, Chicago, IL 60616

M. Saraniti , J. Branlard, Illinois Institute of Technology, Chicago, IL 60616
S. Aboud, Worcester Polytechnic Institute, Worcester, MA 01609-2280
S. Goodnick, Arizona State University, Tempe, AZ 85287

Arizona State University

WPI

Illinois Institute of Technology
Computational Electronic Group

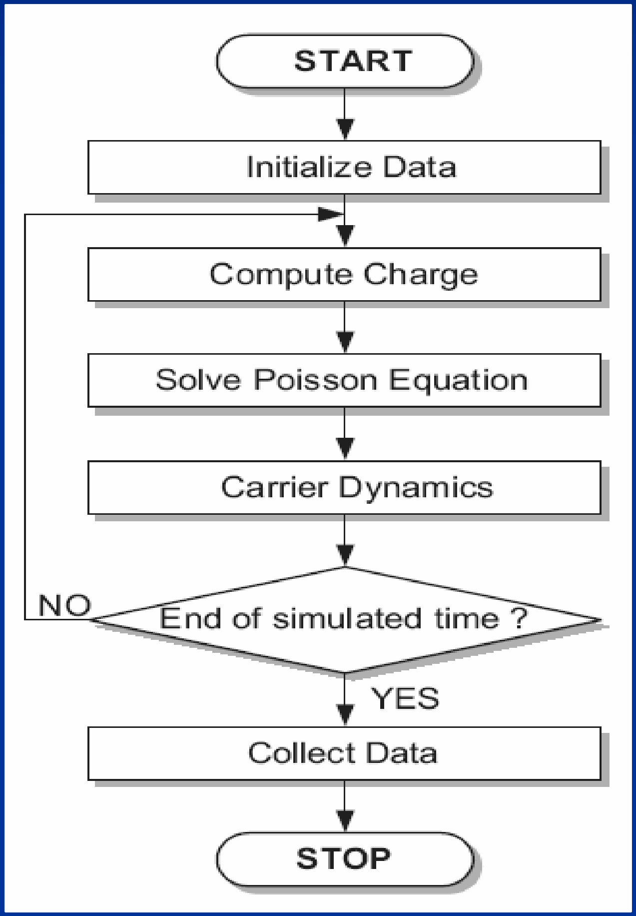
Illinois Institute of Technology
Transforming Lives. Inventing the Future.

Outline

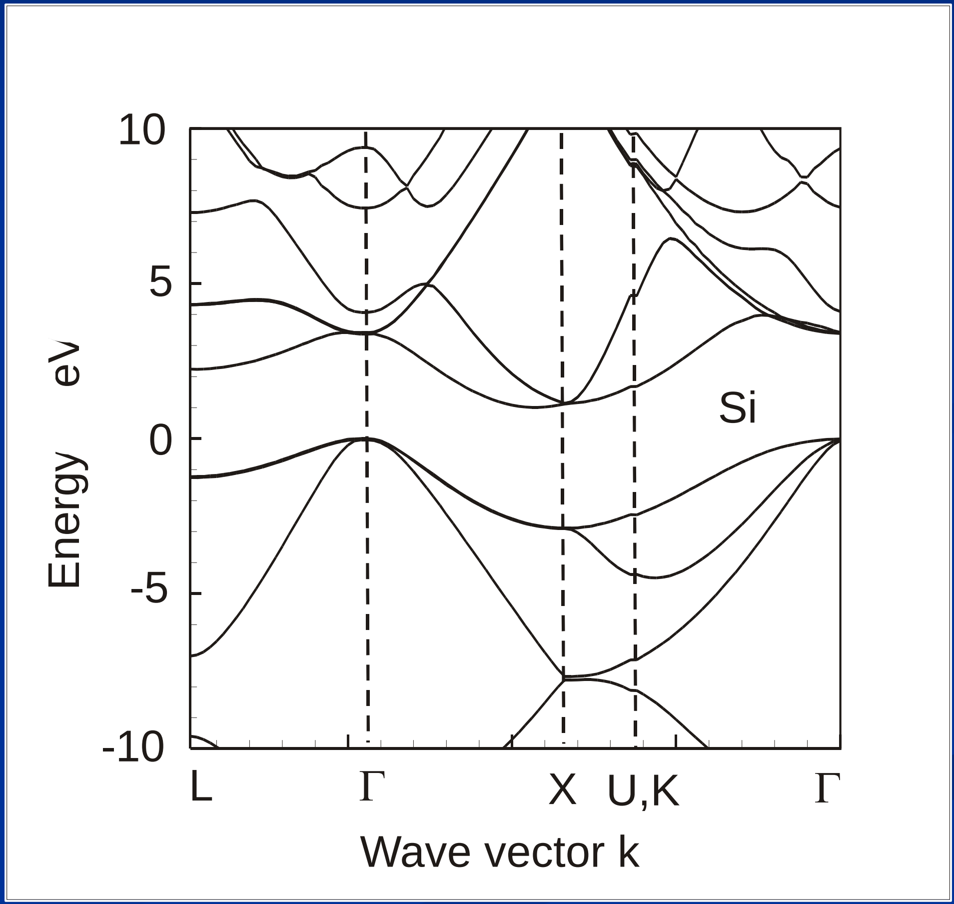
I. Full-band Particle-based Method
II. The Tri-gate devices
III. Device Simulation
IV. Scaling the Tri-gate
V. Frequency Analysis
VI. Future Work

Full-band Particle-based simulation

A simplified flowchart of a particle-based semiconductor simulation technique

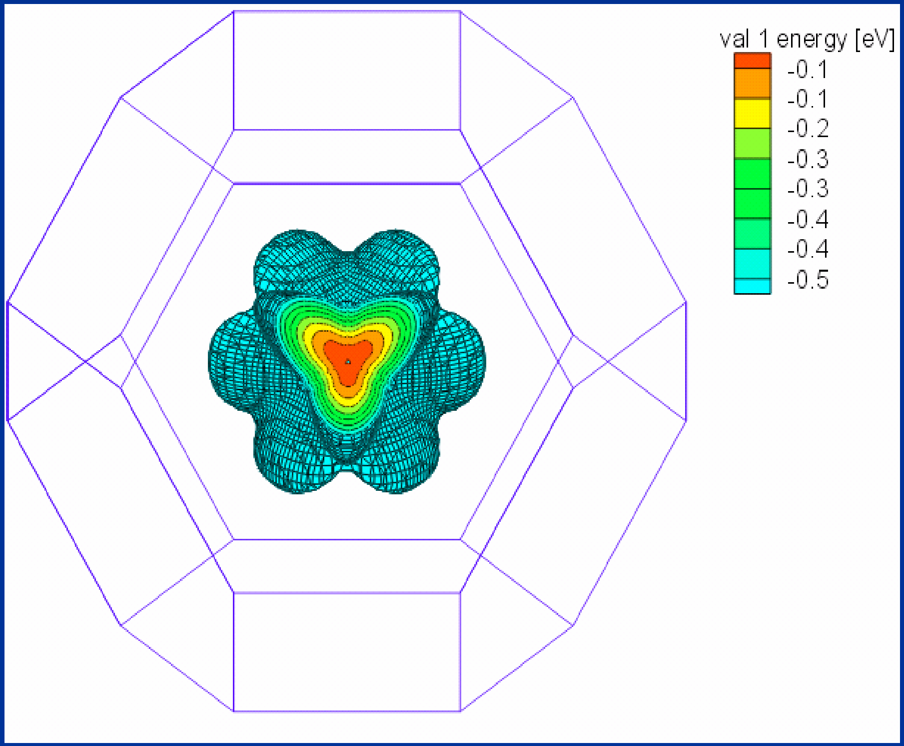


Full-band representation of the Energy-Momentum relation for Si



Hybrid Full-Band EMC/CMC simulator

Full-band representation of electronic dispersion relation for first valence band



EMC

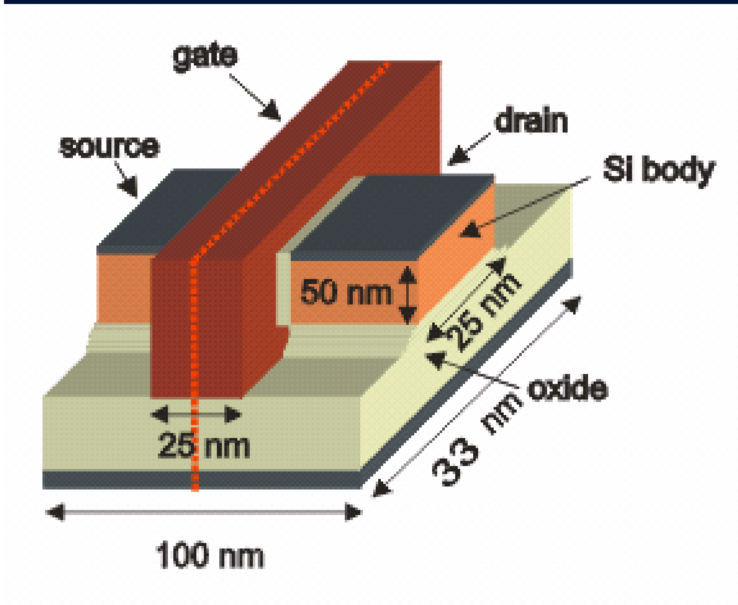
– Regions where total number of scattering events is low
-Saves space

CMC

-Regions where total number of scattering events is high
--Saves time

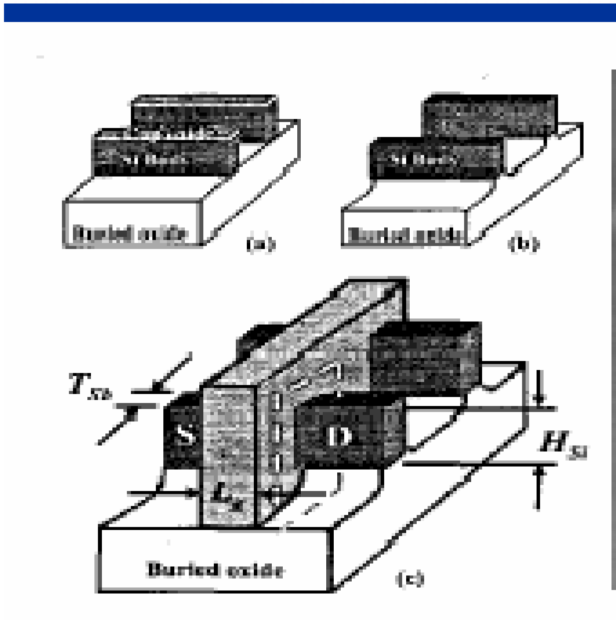
Method used in this work- Hybrid CMC/EMC

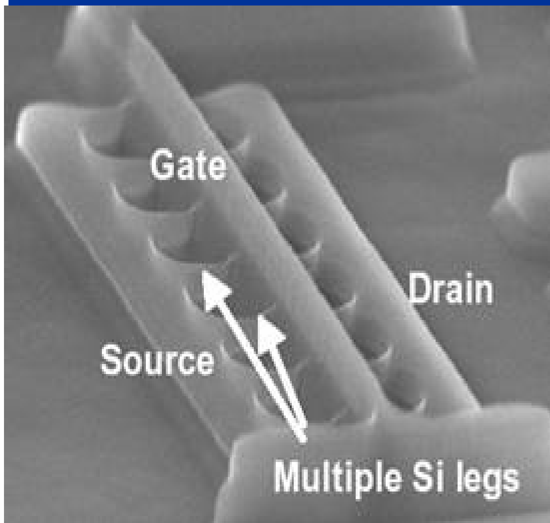
Multiple gate devices: Tri-gate FETs



Promising candidate for future nanometer MOSFET applications

- ✓ **Possess high gate-channel controllability**
- ✓ **Impressive scalability over planar structures**
- ✓ **Achieve high drive currents**

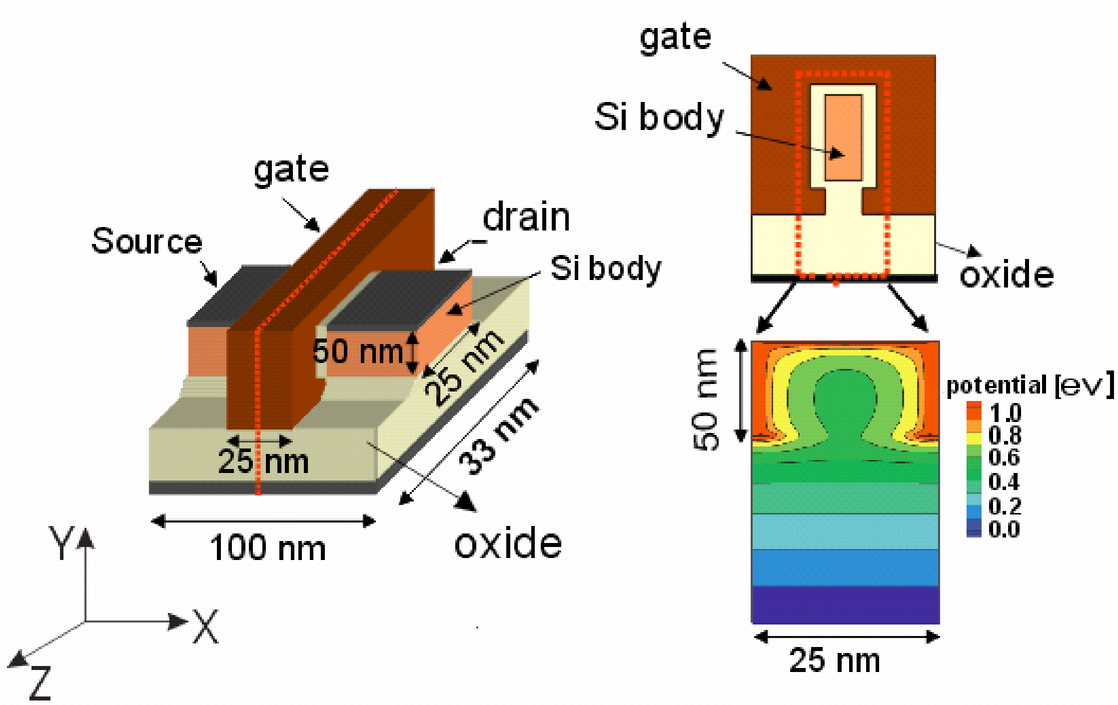


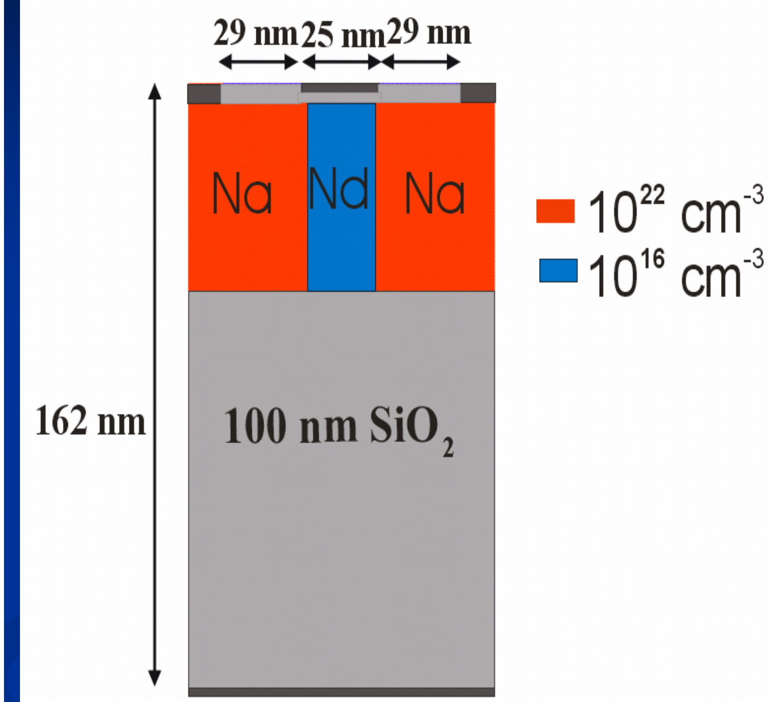


F.L. Yang et al. IEDM Tech. Dig. p.255, 2002

*ITRS`2001 published data

Device Layout of the p-FET





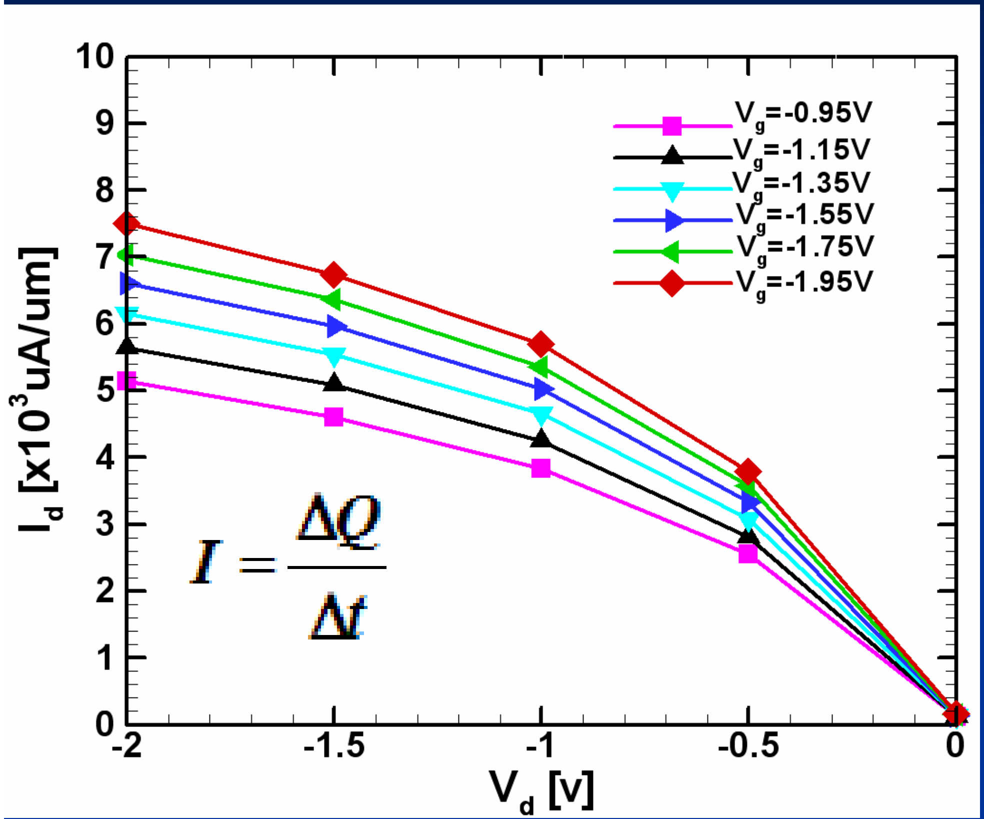
- H_{si} =50 nm , W_{si} =25 nm , L_g=25 nm, doping
- 129 x 65 x 33 inhomogeneous grid
- 260,000 particles
  - ✓P-FETS exhibit record fast transistor switching speed (0.43ps)*

Full-band Particle-based Analysis of
Device Scaling For 3D Tri-gate FETs

*ITRS`2001 published data

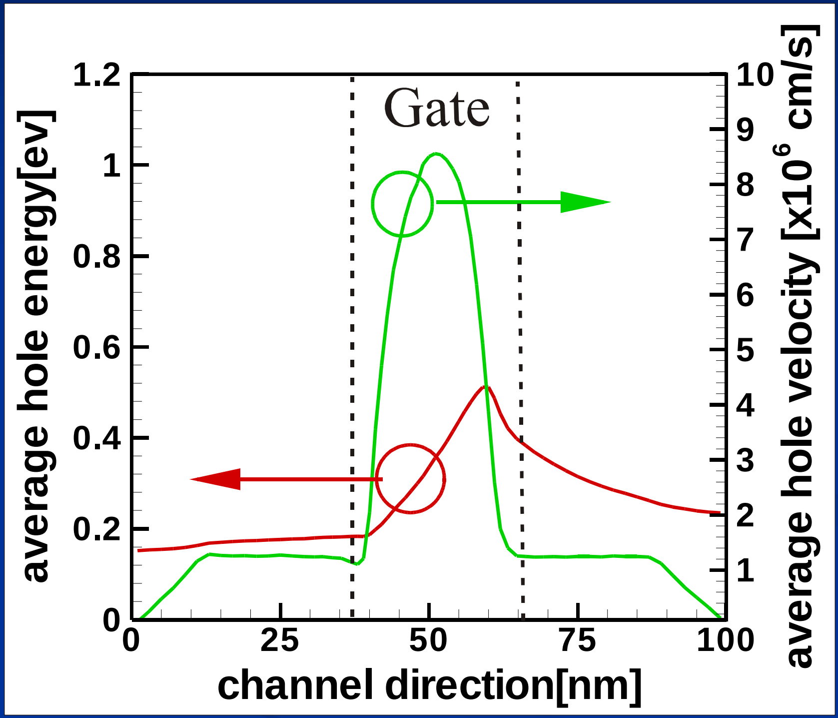
Device Simulation

Current-voltage characteristics



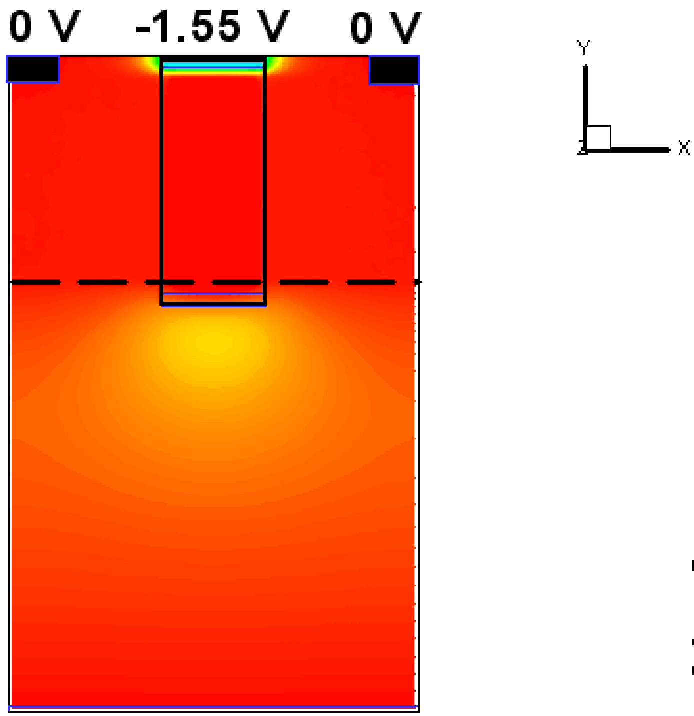
Average energy and velocity

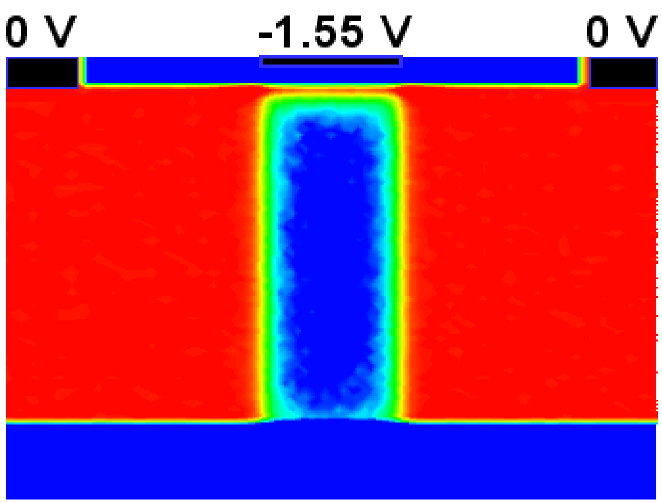
V_g =-1.55 V , V_d =-1.0 V

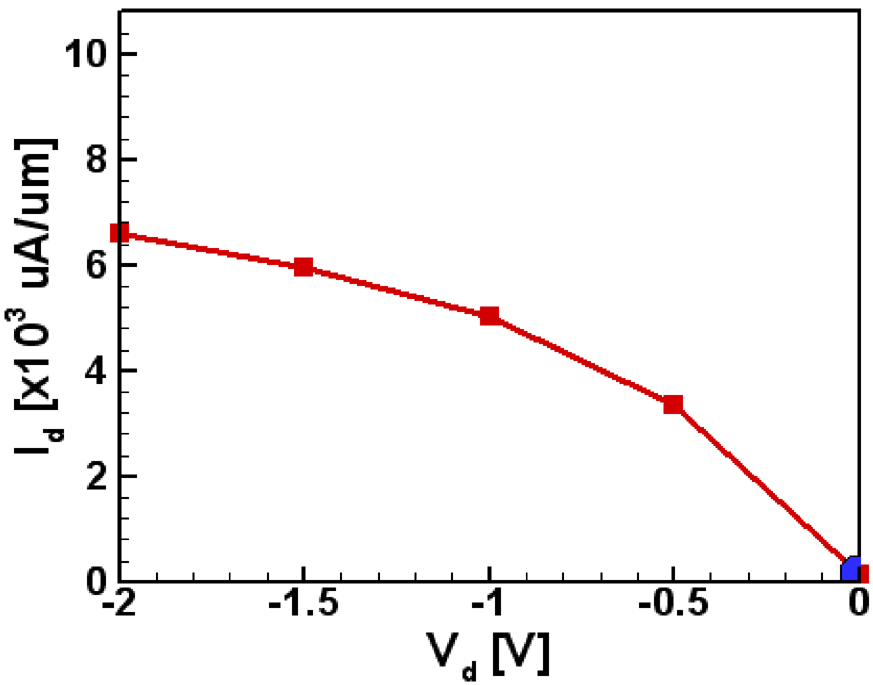


- 260,000 particles
- 24 CPU hrs/ps
- 4 ps/bias point

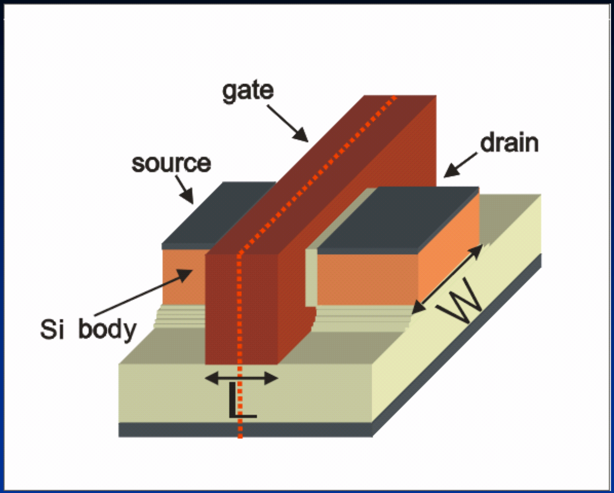
- Velocity overshoot


0 V
-1.55 V
0 V
Y
X


0 V
-1.55 V
0 V


10
8
6
4
2
0
-2
-1.5
-1
-0.5
0
I_d [x10^3 uA/um]
V_d [V]

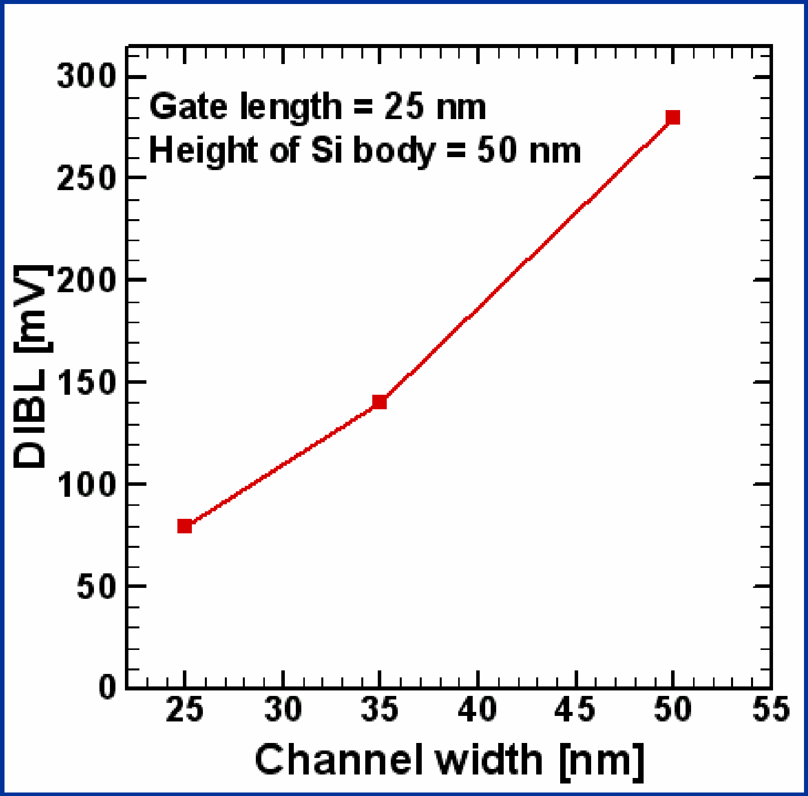
Scaling effects

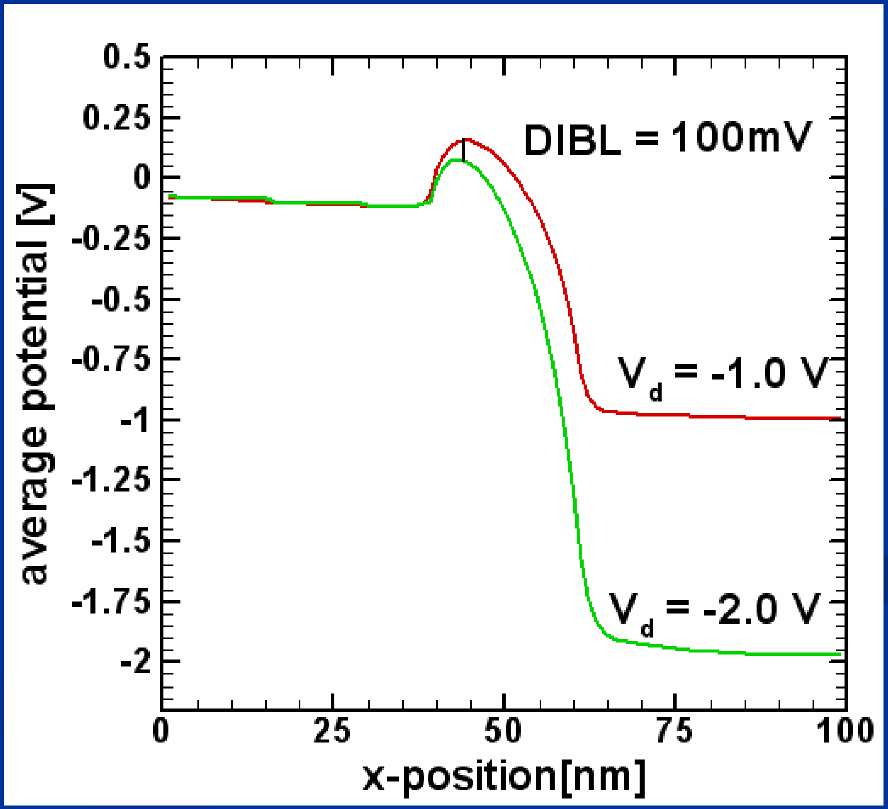


Increase in the channel width -

- DIBL(Drain Induced Barrier Lowering) increases

Calculation of DIBL

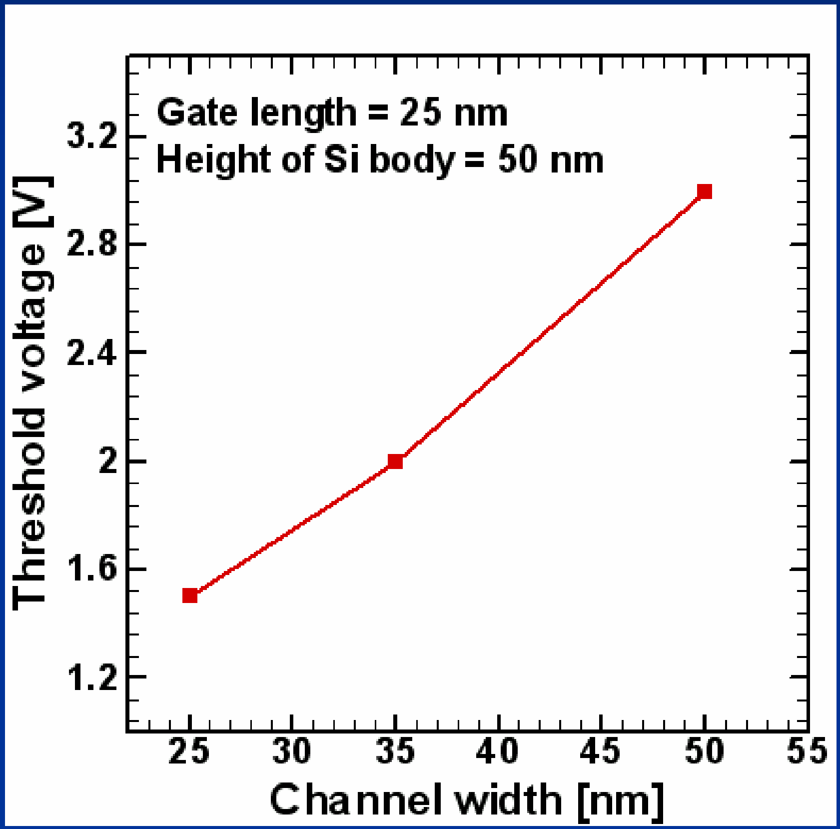




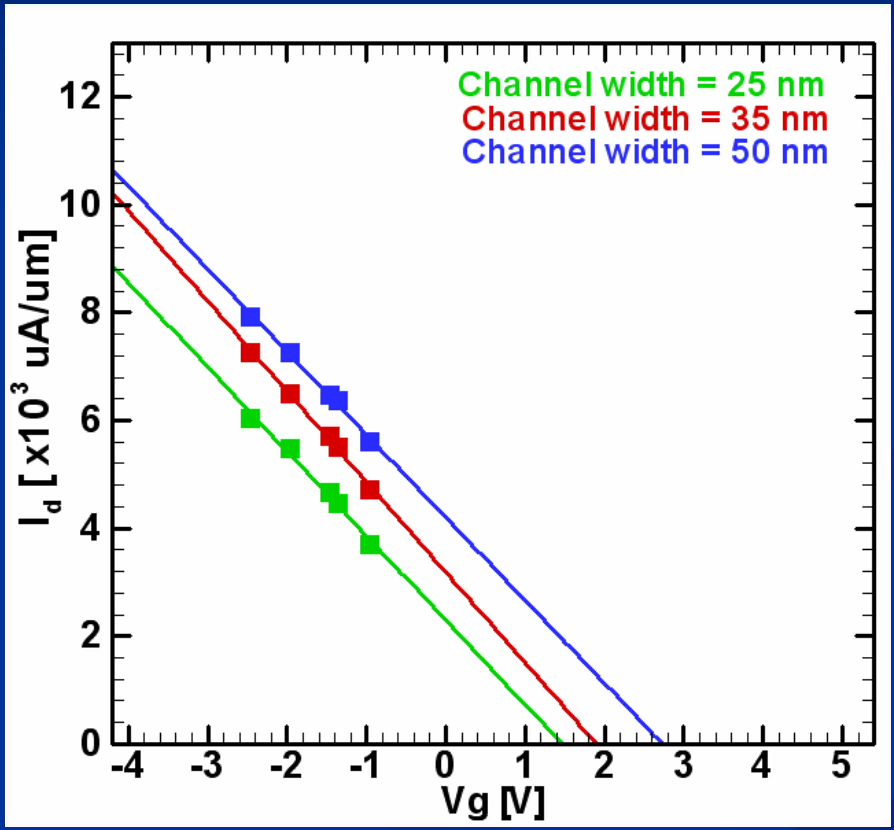
Scaling effects

Decrease in the channel width -

- **Threshold voltage decreases**



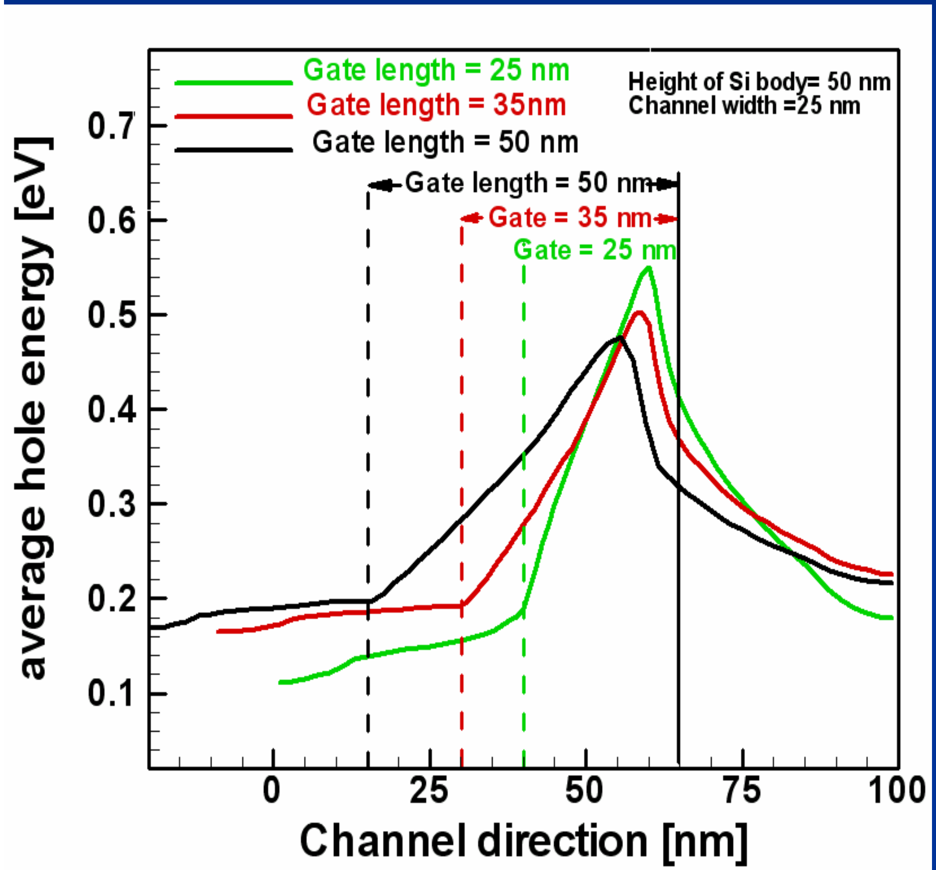
Calculation of Threshold voltage

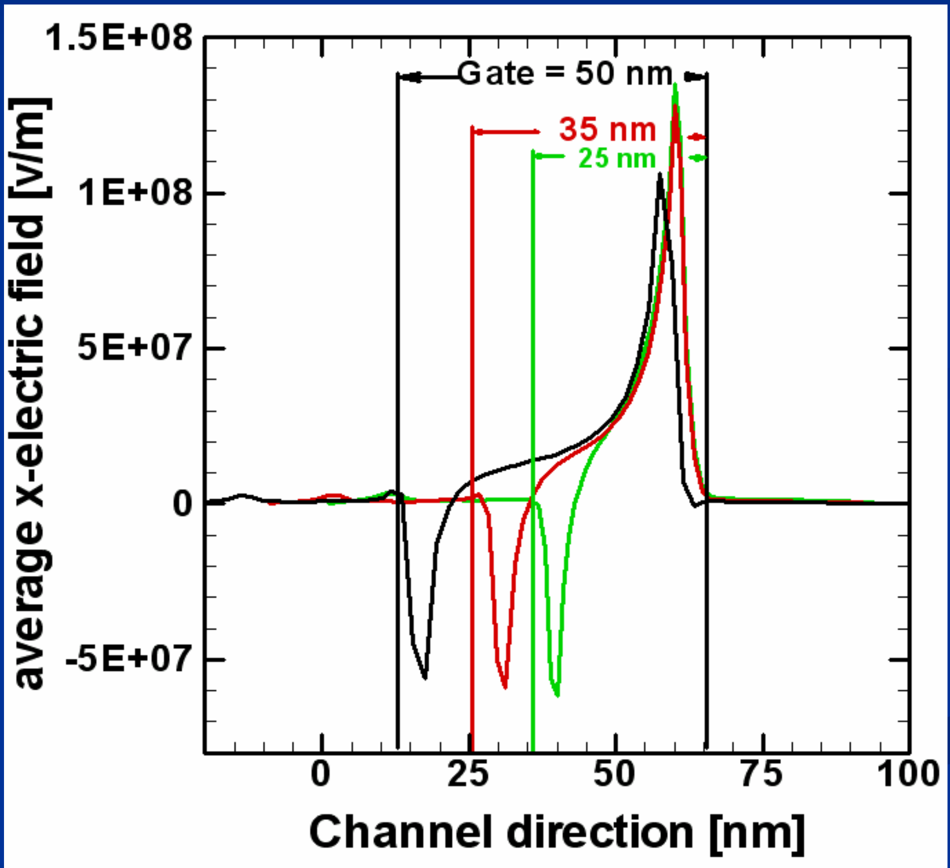


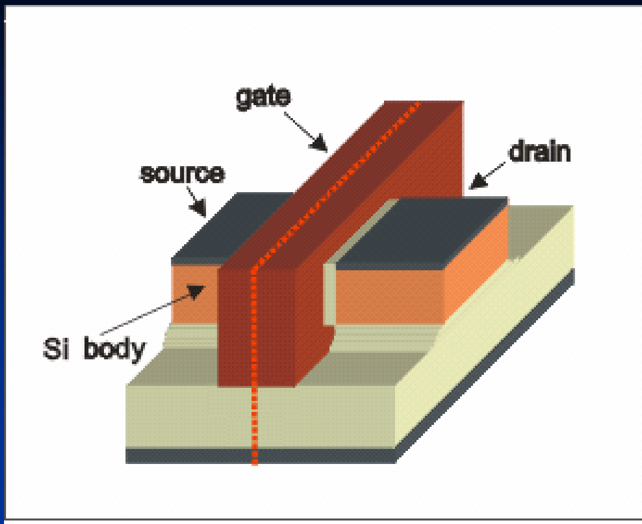
Scaling effects (contd.)

Decrease in the channel length-

- Increase in peak energy
- Increase in electric field

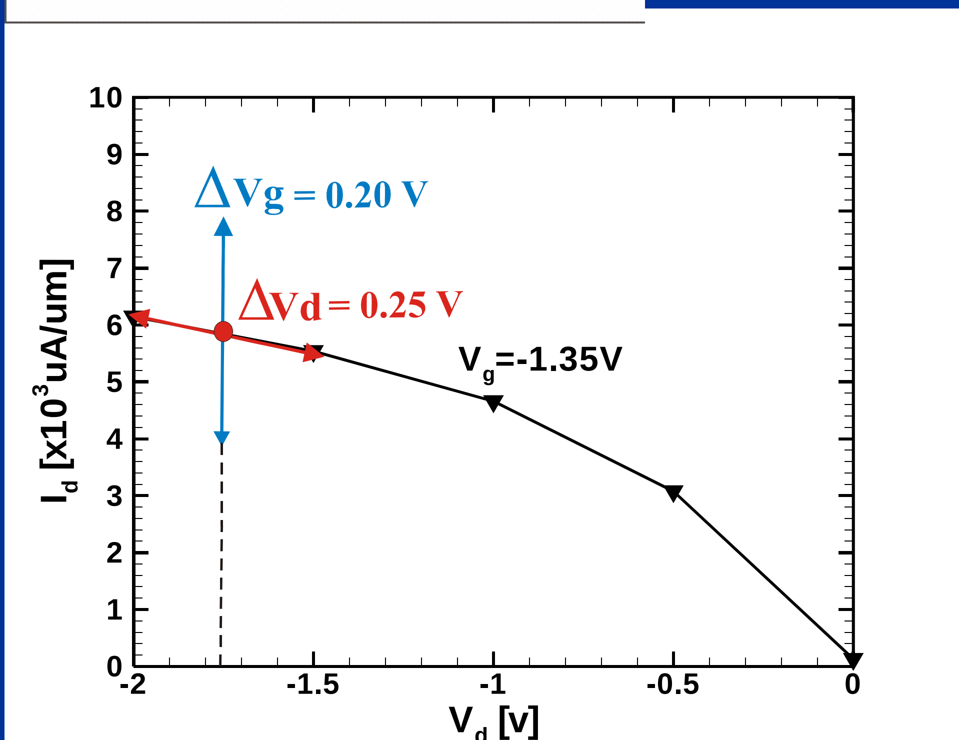






Dynamic Analysis- *To study the effects of scaling the channel width on the dynamic response.*

-- Sinusoidal excitation method



Perturbations are applied successively to the gate and drain electrodes at different frequencies

V_{ds} = -1.35 V
V_{gs} = -1.75 V

Frequency Analysis-Sinusoidal excitation method

Applying Sinusoidal excitation on the drain electrode →

$$Z_{OUT}(\omega) = \frac{v_{ds}(\omega)}{i_d(\omega)} = Y_{22}(\omega)^{-1}$$

Applying Sinusoidal excitation on the gate electrode →

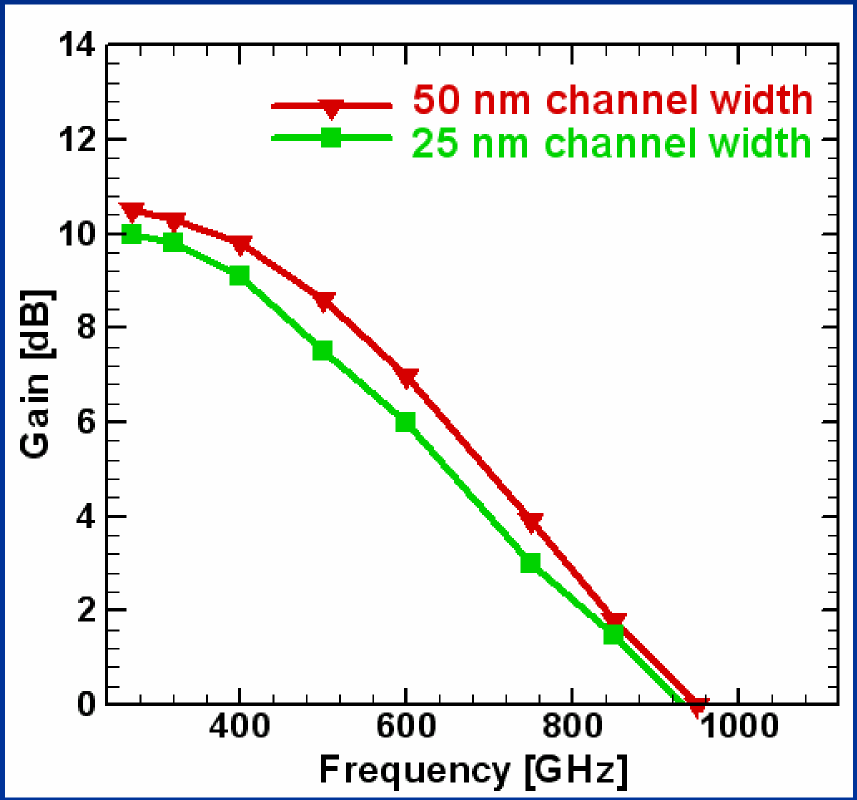
$$g_m(\omega) = \frac{i_d(\omega)}{v_{gs}(\omega)} = Y_{21}(\omega)$$

Gain (G_v) →

$$G_v(\omega) = \frac{v_{ds}(\omega)}{v_{gs}(\omega)} = g_m(\omega) Z_{OUT}(\omega)$$

Dynamic Analysis

Voltage Gain -



Cut-off frequency (G_v =1) :

Channel width 25 nm = 930 Hz
Channel width 50 nm = 950 Hz

--No significant change in cut-off frequency with decrease in the channel width

Current and Future Work

- Further scaling of Tri-gate FETs

  -- Scaling the height of the channel

  Goal- Propose scaling rules/model for tri-gate FETs
- Include Quantum correction
- Account for degeneracy

Thank You!