Simulations of sub-100nm strained Si MOSFETs with high-κ gate stacks

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Outline

- Introduction
- Device structure
  - (Conventional and strained Si *n*-MOSFETs)
- Device Calibration
- High-κ dielectrics
- Results and discussion
- Conclusions

Introduction

- High-κ dielectrics
  - Scaling of MOSFETs beyond the 45nm technology node expected by 2010 (ITRS), requires extremely thin SiO_2 gate oxides (~0.7nm) resulting in intolerably high gate leakage.
  - Maximise gate capacitance:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

  - The leading contenders at present are HfO_2 and Al_2O_3. However, there is a fundamental drawback due to the resulting mobility degradation.

$$t_{high-\kappa} = \left(\frac{\kappa_{high-\kappa}}{\kappa_{ox}} \right) t_{SiO_2}$$

- Strained Si
  - Has already demonstrated significant enhancement for CMOS applications.

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Gate Leakage current density due to gate tunnelling

1.E+05
1.E+04
1.E+03
1.E+02
1.E+01

Jg (A/cm^2)

14
13
12
11
10
9
8
7
6
5
4
3
2
1
0

EOT (A)

EOT

Jg,simulated

Jg,limit

Beyond this point of cross over, oxynitride is incapable of meeting the limit (Jg,limit) on gate leakage current density

2003 2005 2007 2009 2011 2013 2015 2017

Calendar Year

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From ITRS 2003 edition

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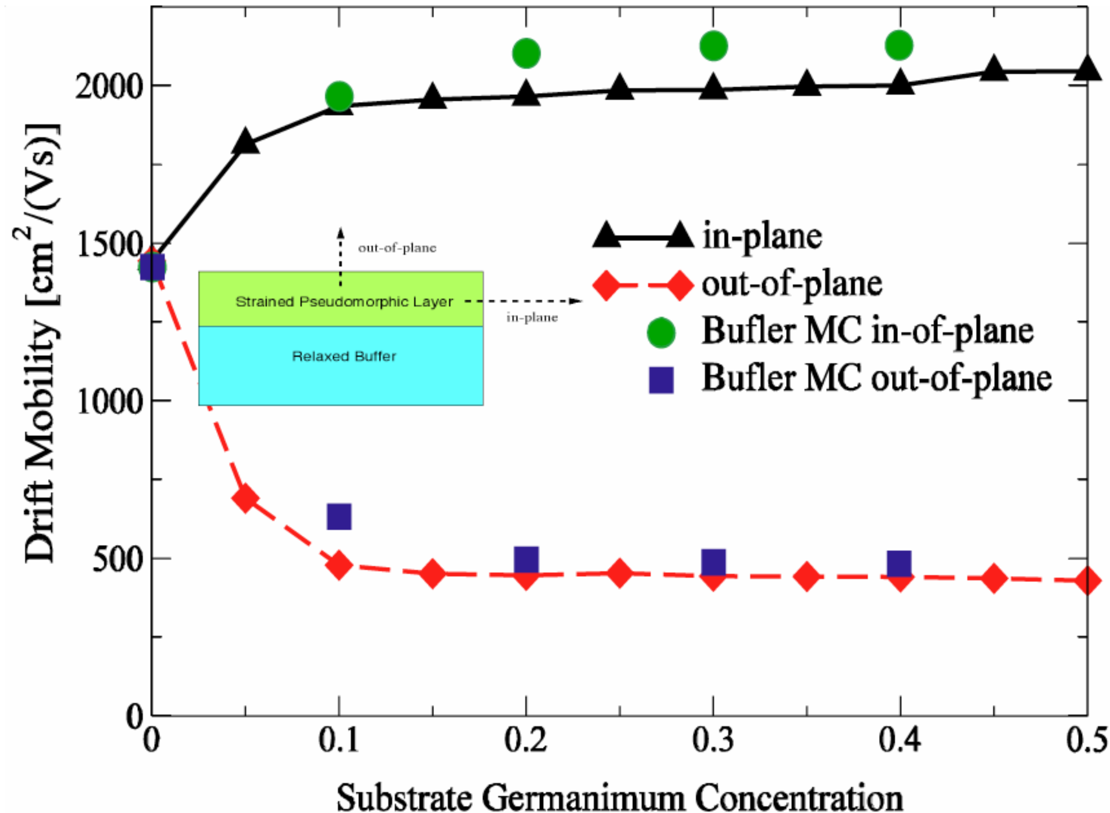
Mobility enhancement in strained Si

Our ensemble Monte Carlo simulator includes all relevant scattering mechanisms:

optical intervalley phonon,
inelastic acoustic phonon,
ionized impurity,

along with interface roughness scattering. The simulator has been thoroughly calibrated for bulk Si transport.



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Monte-Carlo calculation of the low-field *in-* and *out-of-plane* electron mobilities in strained Si as a function of Ge content within the SiGe buffer; inset shows the *in* and *out-of-plane* directions.

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Device Structure Evolution

(a)

Si substrate

(b)

Si substrate

(c)

Relaxed SiGe

Si substrate

(d)

Relaxed SiGe

Si substrate

- Spacer
- N+ poly-Si gate
- SiO_2
- High - κ dielectric

- N+ doping
- Strained Si channel
- Relaxed SiGe buffer
- Si substrate
- Contact

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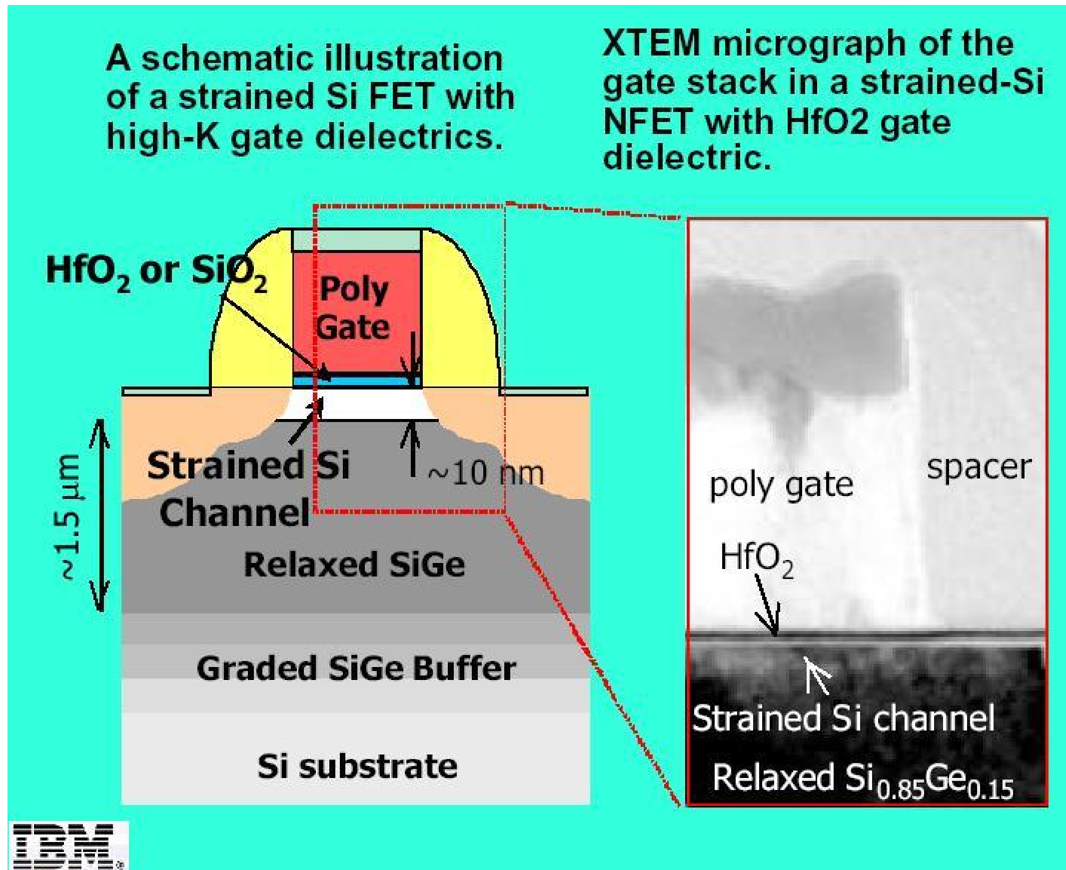
Strained Si with high-κ dielectrics



- IBM demonstrated the high performance of strained silicon (30% enhancement) with low leakage of high-κ insulators (1000× lower leakage) for maximum performance with minimum standby power
- Intel presented their high-κ on strained Si technology at IEDM 2003

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Source: IBM (VLSI 2002)

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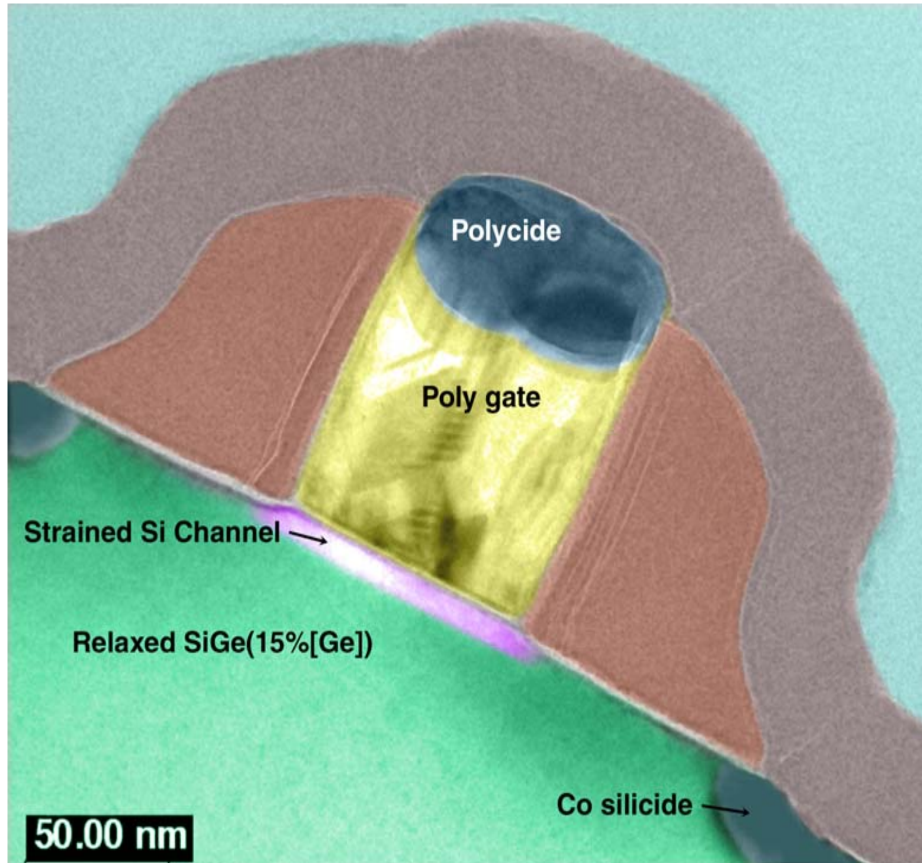
Simulation of 67*nm* IBM Relaxed and Strained Si *n*-MOSFET



Comparison between *n*-type Strained Si and control Si MOSFETs:

- 67nm effective channel length
- Similar processing and the same doping conditions

In the strained Si MOSFET:

- 10nm tensile strained Si layer
- Strained Si on relaxed SiGe (Ge content: 15%)

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K.Rim, et. al., Symposium on VLSI Technology 2001
http://www.research.ibm.com/resources/press/strainedsilicon/

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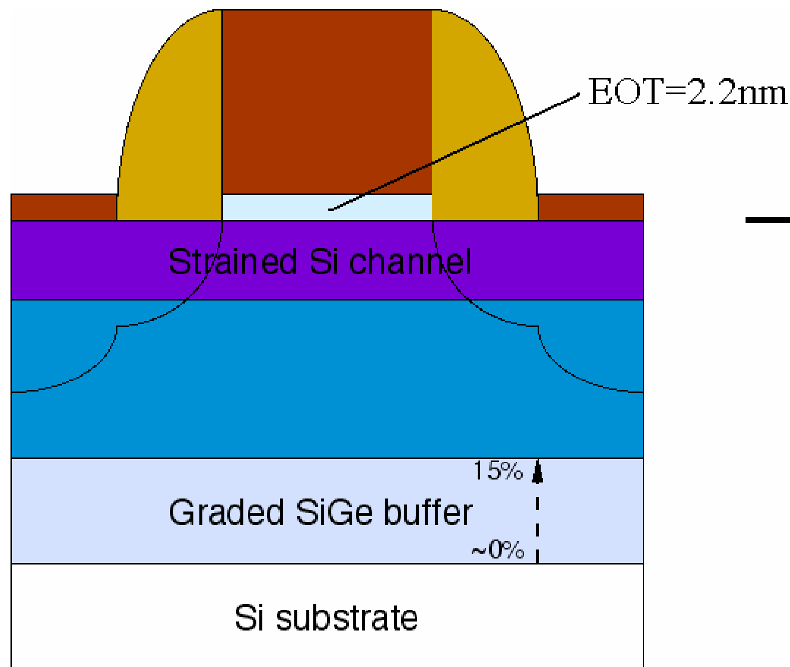
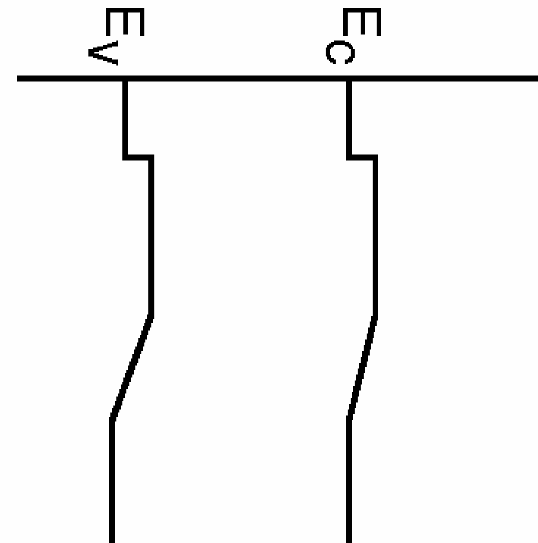
Strained Si *n*-channel MOSFET Structure





Comparison between the *n*-type Strained Si and control Si MOSFETs:

- 67nm effective channel length
- Similar processing and doping conditions
- Oxide thickness, t_{ox} =2.2nm (SiO_2)

For the strained Si MOSFET:

- 10nm strained Si layer thickness
- Strained Si on relaxed SiGe (Ge content: 15%)

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SiGe *n*-MOSFET >35% drive current enhancement (70% high field mobility enhancement)

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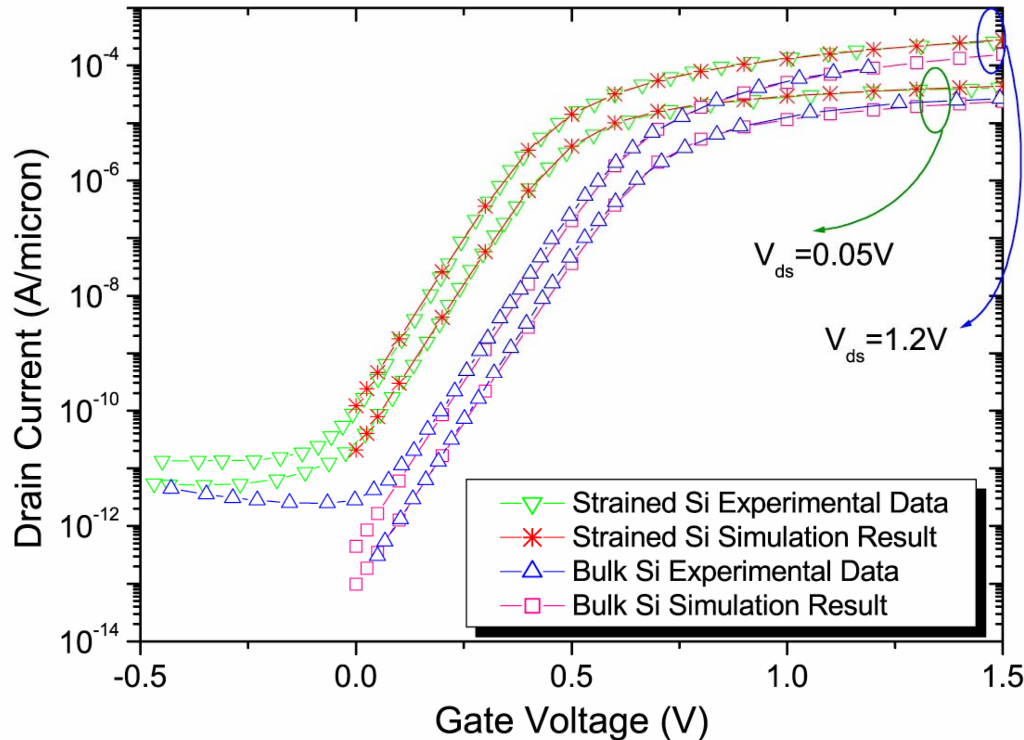
Device Calibration – Drift Diffusion



Drift-diffusion (MEDICI™) device simulations

- Concentration dependent, Caughy-Thomas and perpendicular field dependent mobility models
- Corrected Si/SiGe heterostructure parameters: band gap and band offset, effective mass, DoS and permittivity†

Calibrated I_D-V_G characteristics of the 67nm *n*-type bulk Si and strained Si MOSFETs (experimental data from *Rim VLSI'01*)

† L. Yang, *et al*, 'Si/SiGe Heterostructure Parameters for Device Simulations', to Semiconductor Science and Technology **19**, p. 1174-1182 (2004)

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Device Calibration – Monte Carlo

SSi (Rim VLSI'01)
Si (Rim VLSI'01)
SSi (MC,RMS/CL=0.5/3.0nm)
Si (MC,RMS/CL=0.5/1.8nm)

V_D=0.1V, 1.2V

I_D (A/micron)

V_G-V_T (V)

Calibrated I_D-V_G characteristics for 67nm conventional Si and strained MOSFETs, comparison with experimental data of Rim.

Smoother interface for strained Si/SiO_2 interface.

See L. Yang *et al*, Proceedings of the 5th European Workshop on Ultimate Integration of Silicon (ULIS04), p23-26, IMEC 2004

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Problems associated with high-κ dielectrics

Fixed charge

N_{fix}: fixed charge density

Remote phonon

$t_{high\text{-}\kappa}$: thickness of high-κ

t_{int}: thickness of interfacial layer

Interfacial dipoles

Metal Gate

Δ

Λ

κ_1

κ_2

High-κ

$t_{high\text{-}\kappa}$

t_{int}

Interfacial Layer

Source

e^-

Channel

Drain

Remote surface roughness

Δ: amplitude of roughness

Λ: correlation length

Phase-separation crystallisation

κ_1: κ for crystallised grain

κ_2: κ for amorphous region

Interface trap

N_{it}: trap density

Surface roughness

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High-κ dielectrics

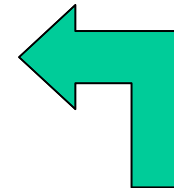
"Ideal" high-κ films: thermally stable, free from electron and interface traps, leakage-free, reliable and reproducible, etc.

Replace SiO_2 →

- Scalability
- Leakage

Quantity/Dielectric	SiO_2	Al_2O_3	HfO_2
ε^0	3.90	12.53	22.00
ε^∞	2.50	3.20	5.03
ω_{TO1} (meV)	55.60	48.18	12.40
ω_{TO2} (meV)	138.10	71.41	48.35
ω_{SO1} (meV)	57.10	53.10	16.70
ω_{SO2} (meV)	140.70	82.33	50.60

Fischetti, JAP'01



{ Ionic polarization
{ Electronic polarization $\propto 1/E_g$

High-κ dielectrics: { High dielectric constant
{ Small bandgap

Highly polarized "soft" metal-oxygen bonds which screen external fields → low energy lattice oscillation (soft - phonon energy)

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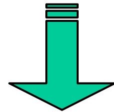
Remote (SO) Phonon Scattering

Coupling strength between the inversion layer electrons and the soft optical (SO) phonons (from the LO modes of insulator) Fröhlich interaction

$$\hbar\omega_{SO}\left[\frac{1}{\varepsilon_s^\infty + \varepsilon_{ox}^\infty} - \frac{1}{\varepsilon_s^\infty + \varepsilon_{ox}^0}\right]$$

Ionic polarization → Static ε_{ox}^0

Electronic polarization → Optical (high frequency) ε_{ox}^∞



SiO_2 – small difference between ε_{ox}^0 and ε_{ox}^∞

High-κ – large difference between ε_{ox}^0 and ε_{ox}^∞

Strong SO phonon scattering degrades the inversion layer carrier mobility within the MOSFET with high-κ gate stacks.

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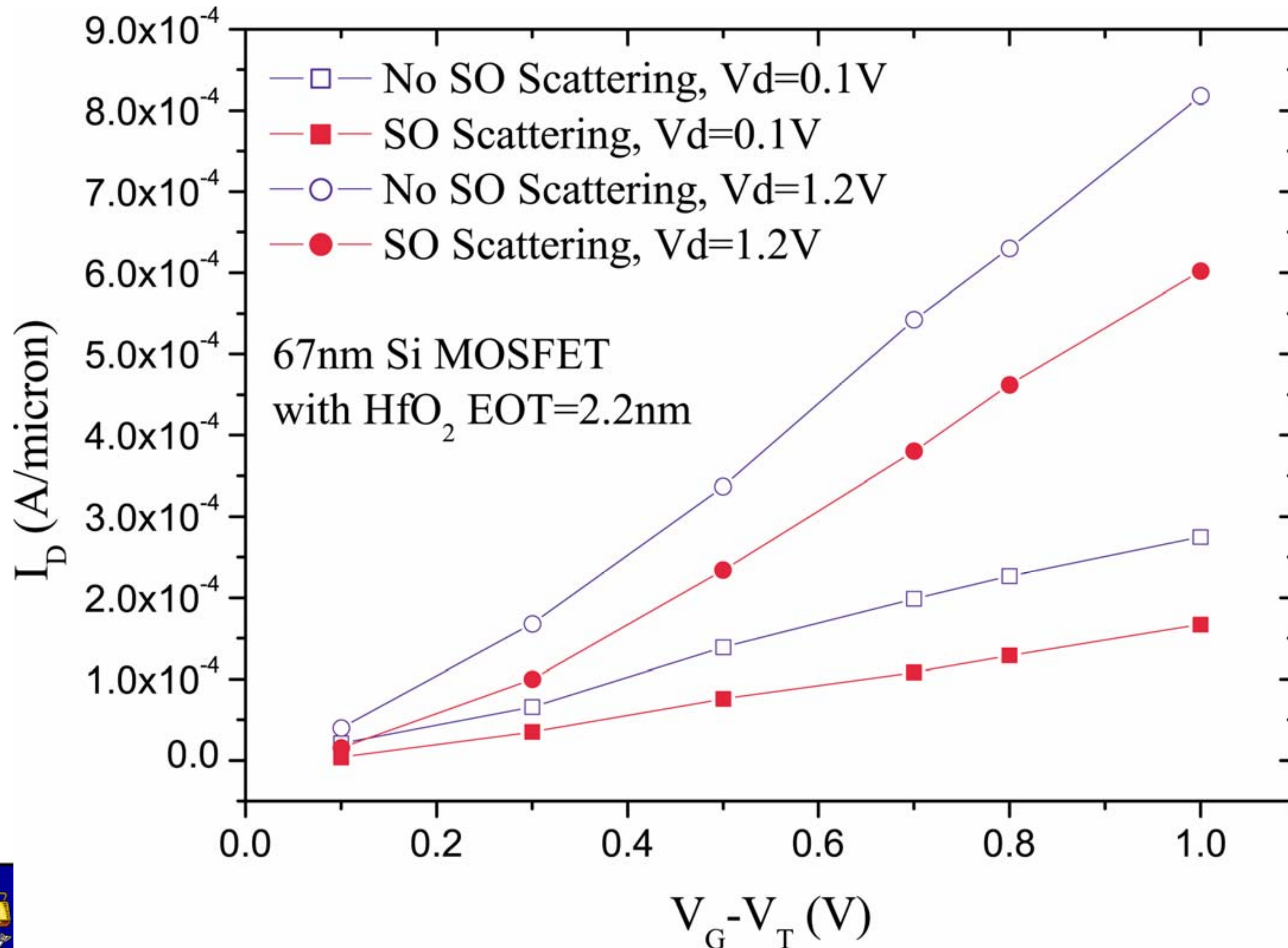
Monte Carlo simulations of Si MOSFET with HfO_2



I_D-V_G characteristics of 67nm *n*-type Si MOSFET, with and without soft-optical phonon scattering from the HfO_2 oxide.

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Monte Carlo simulations of strained Si MOSFET with HfO_2

No SO Scattering, Vd=0.1V
SO Scattering, Vd=0.1V
No SO Scattering, Vd=1.2V
SO Scattering, Vd=1.2V

67nm Strained Si MOSFET
with HfO_2 EOT=2.2nm

I_D (A/micron)

1.4x10^{-3}
1.2x10^{-3}
1.0x10^{-3}
8.0x10^{-4}
6.0x10^{-4}
4.0x10^{-4}
2.0x10^{-4}
0.0

0.2 0.4 0.6 0.8 1.0

V_G-V_T (V)

I_D-V_G characteristics of 67nm *n*-type strained Si MOSFET with and without soft-optical phonon scattering from the HfO_2 oxide.

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Observations

- We observe that those simulations which include soft-optical phonon scattering exhibit a similar percentage reduction for both Si and strained Si *n*-MOSFETs at the same gate over drive V_G-V_T = 1.0V.

- The degradation in the drive current is ~40-50% at V_D=0.1V and ~25% at V_D=1.2V.

- SO phonon scattering decreases at high-drain voltages as the 'Fröhlich' interaction decreases with energy.

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Velocity profile along the channel

Average Channel Velocity (10^7cm/s)

X-direction Dimension (nm)

—□— Strained Si, No SO
—○— Strained Si, SO
—△— Si, No SO
—▽— Si, SO

HfO_2 EOT=2.2nm
L_{eff}=67nm

V_G-V_T=1.0V
V_D=1.2V

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Average channel velocities for the 67nm *n*-type bulk and strained Si MOSFETs, with and without soft-optical phonon scattering from the HfO_2 gate stack.

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Monte Carlo simulations of Si MOSFET, with Al_2O_3

Strained Si, No SO
Strained Si, SO
Si, No SO
Si, SO

Al_2O_3 EOT=2.2nm
L_{eff}=67nm, V_D=1.2V

I_D (A/micron)

V_G-V_T (V)

I_D-V_G characteristics of 67nm *n*-type Si MOSFET, with and without soft-optical phonon scattering, from the Al_2O_3 oxide.

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Impact of high-κ on Strained Si

Universal Mobility

HfO_2/Strained Si with TiN metal gate

SiON/Control Si

HfO_2/Control Si with TiN metal gate

HfO_2/Control Si with Poly Si gate

Inversion Electron Mobility (cm^2/V.s)

500
400
300
200
100
0

0.0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6

Electric Field (MV/cm)

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Source: Intel, IEDM 2003

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Conclusions

- We have investigated the impact on the performance degradation in sub 100nm *n*-MOSFETs due to soft-optical phonon scattering in the presence of high-κ dielectrics HfO_2 and Al_2O_3.
- A device current degradation of around 25% at V_G-V_T=1.0V and V_D=1.2V is observed for conventional and strained Si devices with a 2.2nm EOT HfO_2. Correspondingly a current degradation of around 10% is observed for conventional and strained Si devices with a 2.2nm EOT Al_2O_3.
- Our results indicate that the performance degradation associated with high-κ gate stack MOSFETs can be compensated by the introduction of strained Si channels.
- The infancy of high-κ gate fabrication techniques means that overall performance degradation associated with high-κ gate dielectrics is expected to be worse than the predictions here.

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